apple® service

# APPLE III
# SERVICE
# REFERENCE
# MANUAL

apple computer inc.

To the Reader,

This manual was developed for all the A/// Service Technicians at our Level II Regional Service Center. The intent of this book is to help you understand and repair the Apple ///. The book is partitioned into two sections: Theory of Operation and Servicing Information. There is sufficient information in this manual so that an inexperienced technician can be productive in a short time. This manual should help you understand and appreciate the Apple ///.

In Appreciation:

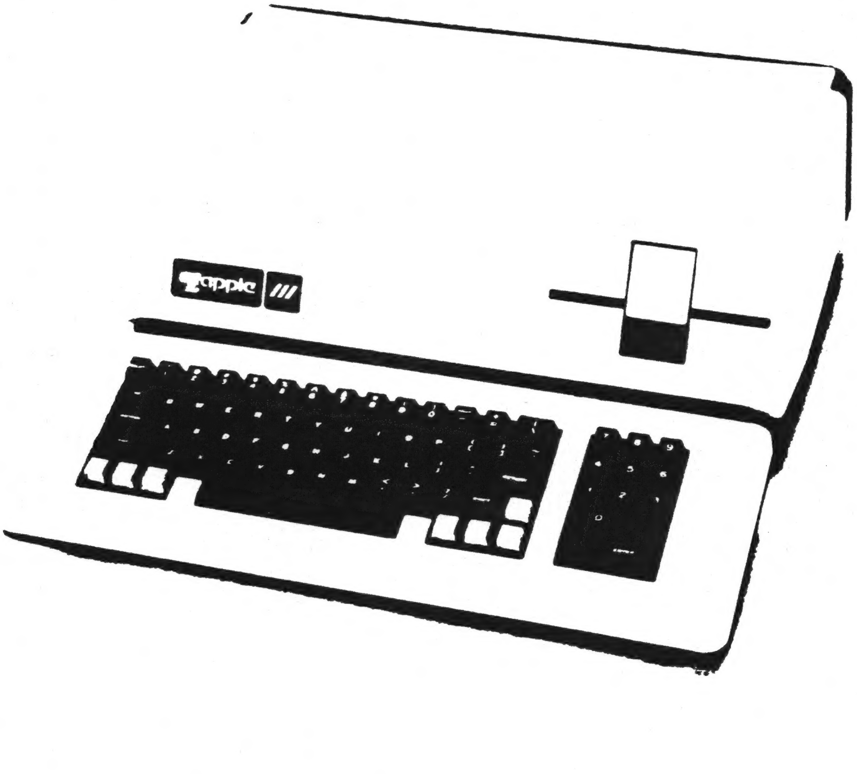
Although many people have helped me with this manual I wish to particularly thank the following people for their contribution to this manual:

Bill Holman
Wendell Sanders
Mike Fallon
Rick Hoiberg
Ed Goodwin
Sandy Sanford
Peter Quinn

Thanks!

Bob Cummings
Bob Cummings

apple service



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# MANUAL

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# INTRODUCTION

## GENERAL DESCRIPTION

The Apple /// is a personal computer for the professional. It has the capabilities to run very involved programs since it can have up to 256K of RAM. The overall unit has been designed to incorporate the best features and options that make it a complete personal computer. The Apple ][ emulation mode allows users to run most Apple ][ software. However, minor modifications may be required for some Apple ][ programs or other peripheral devices.

The base system has a full ASCII keyboard which includes a 13-key numeric key pad with two special function keys. There are four cursor control keys. The A/// has two special repeat features: 1) each key repeats when held depressed, and 2) a high-speed repeat is activated with the Solid Apple key. It's typewriter style keyboard is sculptured for maximum typing speed and accuracy.

The Apple /// has a built-in disk drive (140K bytes) and controller which is capable of supporting three additional external drives without additional interfacing. One interesting feature is that the two drives may be on at the same time. This increases the disk-to-disk transfer effectiveness. The Apple /// can also be used with "Profile"- Apple's 5 Megabyte hard disk for mass data storage.

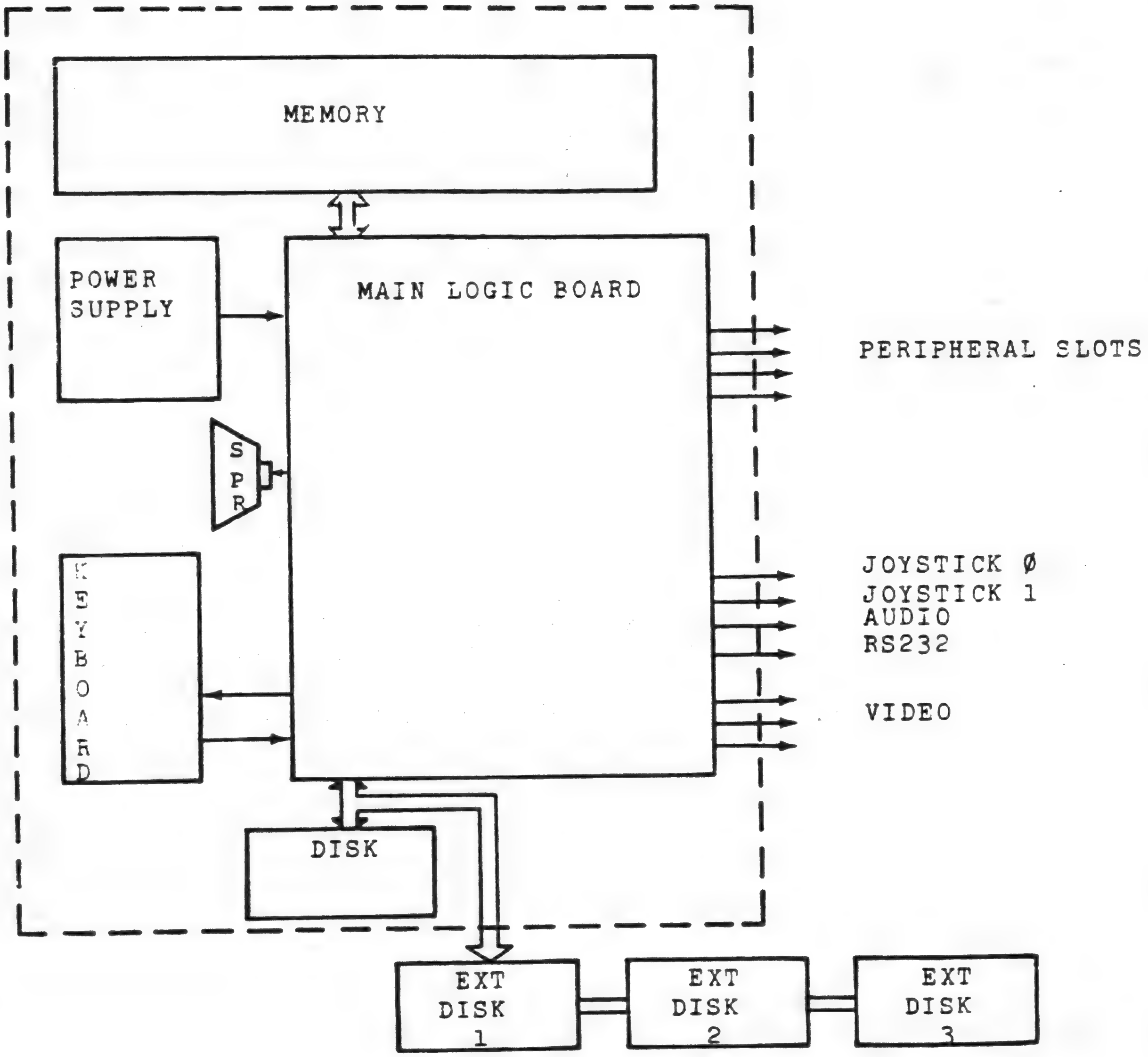
A built-in RS-232 port, located on the back panel, allows you to connect the Apple /// to letter quality printers, high-speed data collection devices, modems, and other serial input/output devices using RS-232-C protrocol. The A/// has two joystick ports for games, sophisticated cursor control, or silentype operation.

The Apple /// has 8 different modes of video operation. B/W Text in 40 and 80 column, a 40 column 16 color text mode (where the foreground and background of each character can be defined). The Apple ][ graphics modes are duplicated and there are three more graphics modes: a super black and white Hi-Res, 16 color Hi-Res, and 16 color medium resolution graphics. The eigth mode is actually a utilizatin of the color text mode where the user defines the character image and builds video images with these "character sets". Since the video character generator is RAM, not ROM, as in the Apple ][, it provides the user with the capability of defining character sets to display whatever the user wants. Three video outputs are provided at the back panel; these are black and white, NTSC color composite, and RGB video for exceptional color purity and resolution.

The Apple ///'s Central Processing Unit (CPU) can be "interrupted" by peripheral devices whenever they require CPU control. Alternatively the CPU can poll the devices to determine which needs attention, thereby minimizing the software required for peripheral control.

There are more features in the Apple /// such as, a built-in clock/calender, a hardware beeper to simplify programming, a six-level D/A converter for more

# A III SYSTEM BLOCK DIAGRAM


MEMORY
POWER SUPPLY
MAIN LOGIC BOARD
PERIPHERAL SLOTS
SPR
KEYBOARD
JOYSTICK 0
JOYSTICK 1
AUDIO
RS232
VIDEO
DISK
EXT DISK 1
EXT DISK 2
EXT DISK 3

# A III SYSTEM BLOCK DIAGRAM

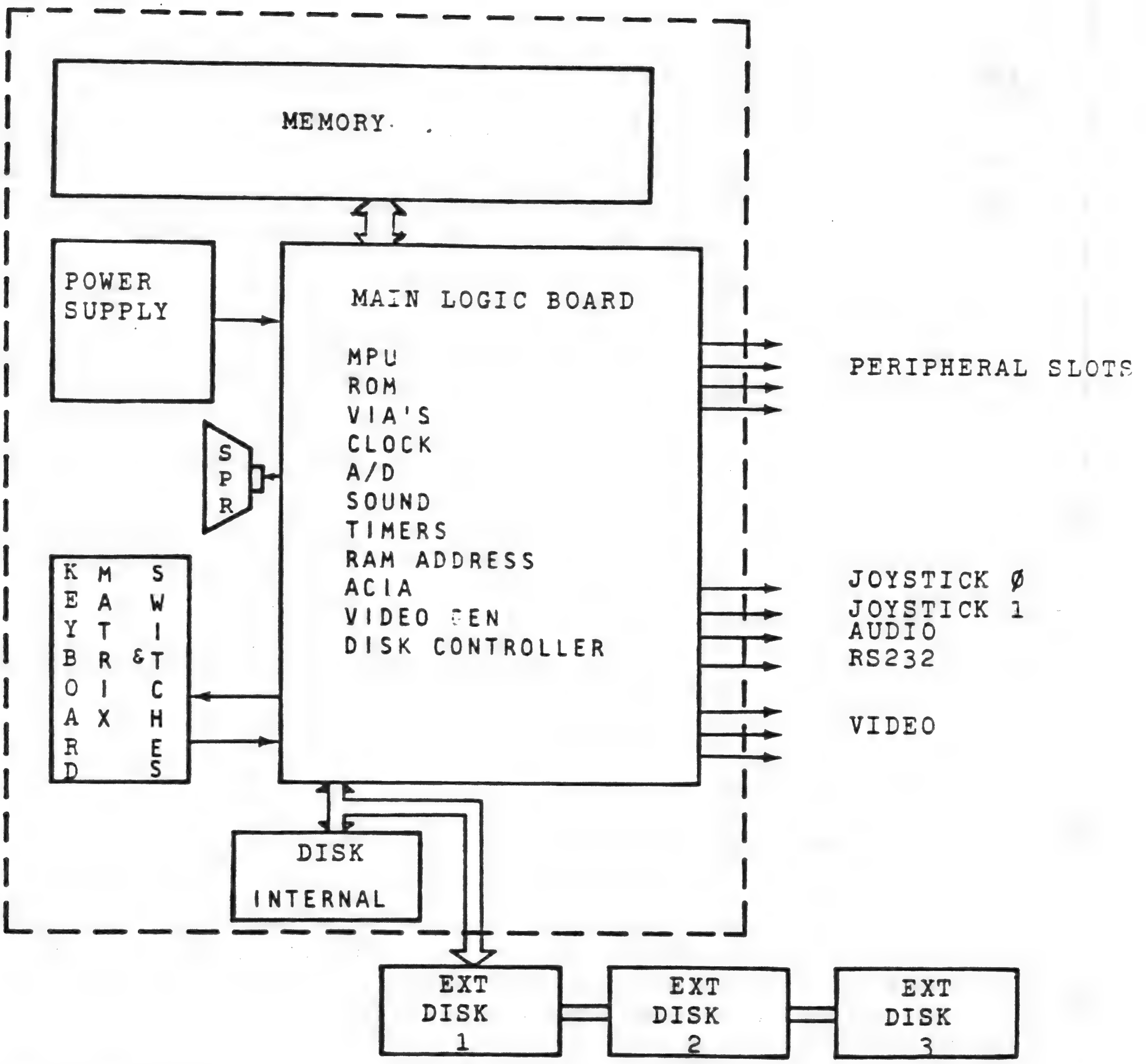

MEMORY
POWER SUPPLY
MAIN LOGIC BOARD
MPU
ROM
VIA'S
CLOCK
A/D
SOUND
TIMERS
RAM ADDRESS
ACIA
VIDEO GEN
DISK CONTROLLER
SPR
KEYBOARD
MATRIX
&
SWITCHES
DISK INTERNAL
PERIPHERAL SLOTS
JOYSTICK 0
JOYSTICK 1
AUDIO
RS232
VIDEO
EXT DISK 1
EXT DISK 2
EXT DISK 3

FIG 1.1

## DEFINITIONS

MPU - MICROPROCESSOR
ROM - READ ONLY MEMORY
VIA - VERSATILE INTERFACE ADAPTER: A SPECIAL PURPOSE PROCESSOR
ACIA - ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER PROVIDES RS232 COMMUNICATIONS CAPABILITY.
A/D - ANALOG TO DIGITAL CONVERTER

complex tone generation, and the duplication of the speaker function of the Apple ][.

As you can see there are many onboard features that would fully load an Apple ][, yet the Apple /// has four expansion slots for additional user interfacing. As you read this document and learn how it works, you will appreciate its capabilities, design, and usefulness.

## SIMPLIFIED FUNCTIONAL DESCRIPTION

The Apple /// is not an easy machine to understand. It has been designed to emulate the Apple ][ and has done many operations in a different manner, while adding many enhancements which contribute to its complexity. To understand the system structure it is best to start building functional blocks and gain an understanding of each separately, and then comprehensively.

There are five major parts (modules) to the Apple ///. These parts are:

1) Main Logic PCB - this board functions primarily as a processor and device controller. Many functions are integrated into the board, including the disk controller.

2) Memory PCB - this board stores data/programs temporarily (until power is removed).

3) Keyboard PCB - this is the primary input device provided to the user.

4) Disk Drive - Mass storage device for storing data.

5) Power Supply - provides the voltages and regulation required to keep everything else working.

## THE MAIN LOGIC BOARD

The Main Logic Board is easily identified by its large size and mass quantities of integrated circuits (IC's).

Referring to the block diagram of Figure 1.1 we encounter the microprocessor (MPU), Boot/Monitor ROM, address decode/select circuitry, the Versatile Interface (VIA) containing the bank switch register and the sound register, the VIA containing the environmental and zero page registers, the Asynchronous Communications Interface Adapter (ACIA), analog to digital circuit (joystick inputs), the expansion I/O slots, disk controller, keyboard encoder, video generator, RAM, RAM address circuits, and the system and video timing circuits. Whooo, now you see why it's so big!

Figure 1.1 shows the Apple /// in it's simplest form and presents its expanded I/O capability. On the other hand, the System Functional Block Diagram displays the system in more detail and presents a sophisticated system using some highly unique designs. Some definitions have been provided for some of the terms used in the block diagram.

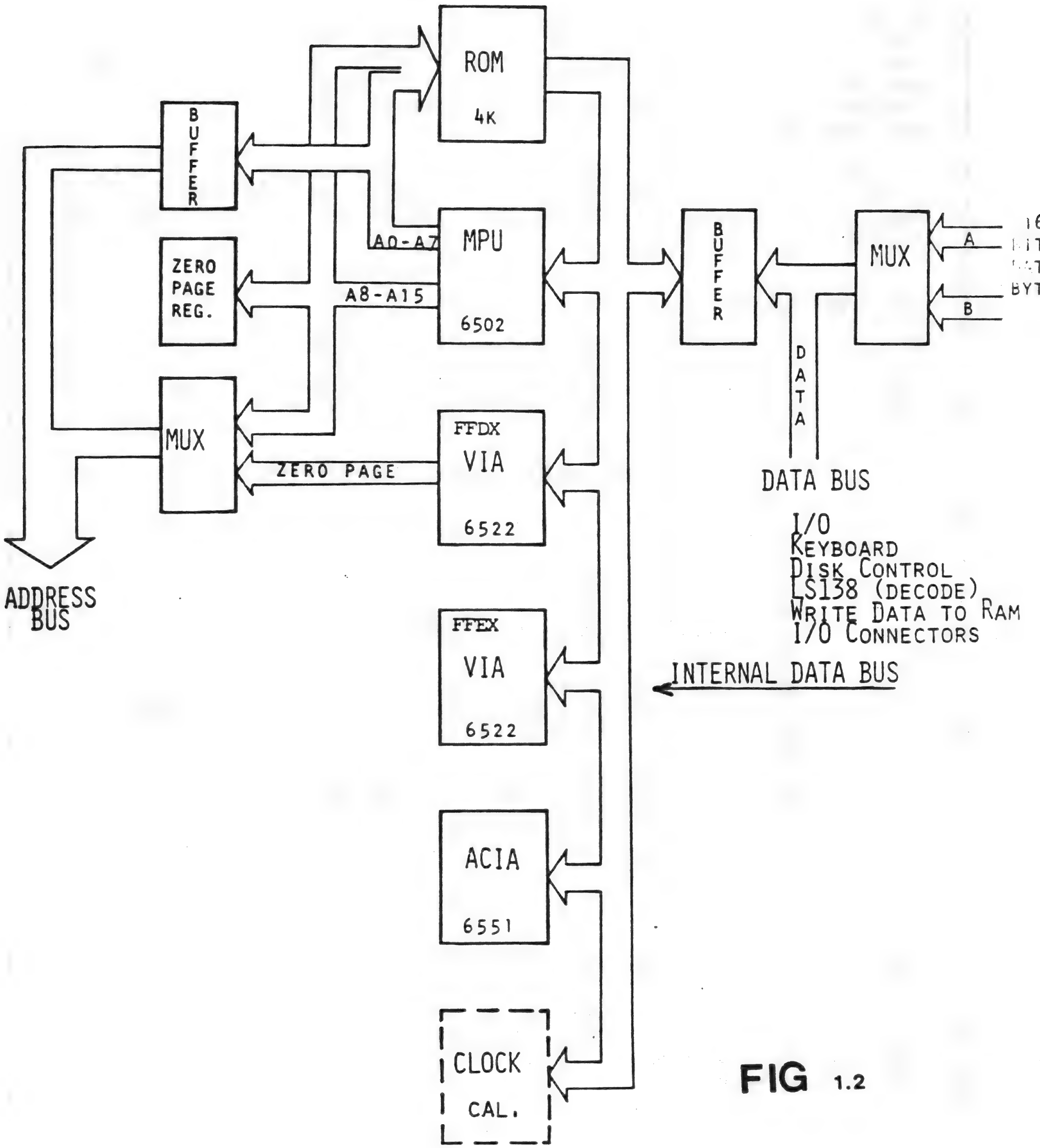

ROM
4K
BUFFER
ZERO PAGE REG.
MUX
ADDRESS BUS
MPU
6502
A0-A7
A8-A15
FFDX
VIA
6522
ZERO PAGE
FFEX
VIA
6522
ACIA
6551
CLOCK
CAL.
BUFFER
DATA
MUX
A
B
16
BIT
BYT
DATA BUS
I/O
KEYBOARD
DISK CONTROL
LS138 (DECODE)
WRITE DATA TO RAM
I/O CONNECTORS
INTERNAL DATA BUS

FIG 1.2

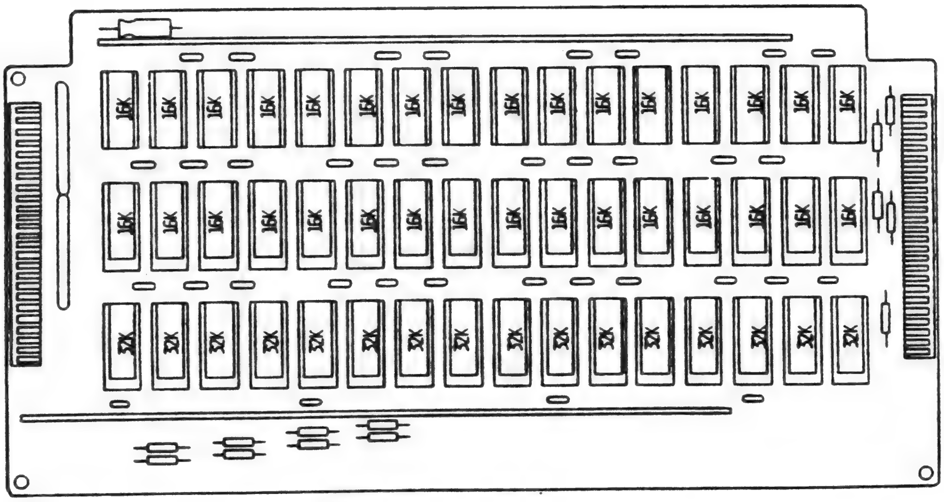
It is best to think of the Apple /// processor as more than just the MPU chip. The processor/controller is actually comprised of many components. The most significant of these are the MPU and the two VIA's. Because of the system's complexity and memory size, the MPU must have extended addressing. Extended addressing is accomplished thru bank switches, environmental register, and a zero page register.

The Apple /// system is interrupt driven. In order to efficienctly use processing time, only those devices that allow programs access to the processor are serviced. In fact the processor can even totally mask (disable) the reset key.

## THE MEMORY BOARD

The other PCB in the Apple /// is the memory board. It is mounted on the Main Logic Board by two rows of pin connectors. There are two distinct types of memory boards. The early memory board version is commonly refered to as the 12V Memory Board. Below is an illustration of this board.

THE 12 VOLT MEMORY BOARD (128K CONFIGURATION)


16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
16K
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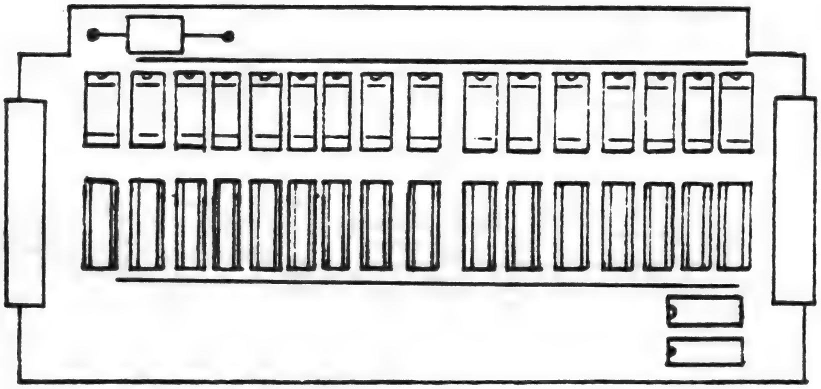
16K
16K
16K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K
32K

With the correct Main Logic Board configuration, this board can have up to 128K RAM (without modification). The board uses 16K and 32K RAM chips.

The latest memory board version is called the 5 Volt Memory Board. This board, illustrated in the accompanying pages, can be configured for 128K or 256K RAM. The 5 Volt Memory Board, however, requires the correct Main Logic Board configuration.

## THE 5 VOLT MEMORY BOARD (128K CONFIGURATION)



## THE KEYBOARD PCB

This has to be one of the nicest keyboards around. The sculptured keys are a delight to touch. The Apple /// does not have an on board keyboard encoder - the keyboard encoder is on the Main Logic Board. The keyboard is basically a matrix of switches. The keyboard is connected by means of a 26 pin ribbon cable to the Main Logic Board.

## THE DISK DRIVE

The disk drive is similiar to the Disk ][. The major difference between the Disk ][ and the Apple /// drive are the door, the bezel, and the Analog Card. Disk switch detection circuitry has been added to the Disk /// Analog Card. Through daisey-chaining you can have up to three (3) external disk drives.

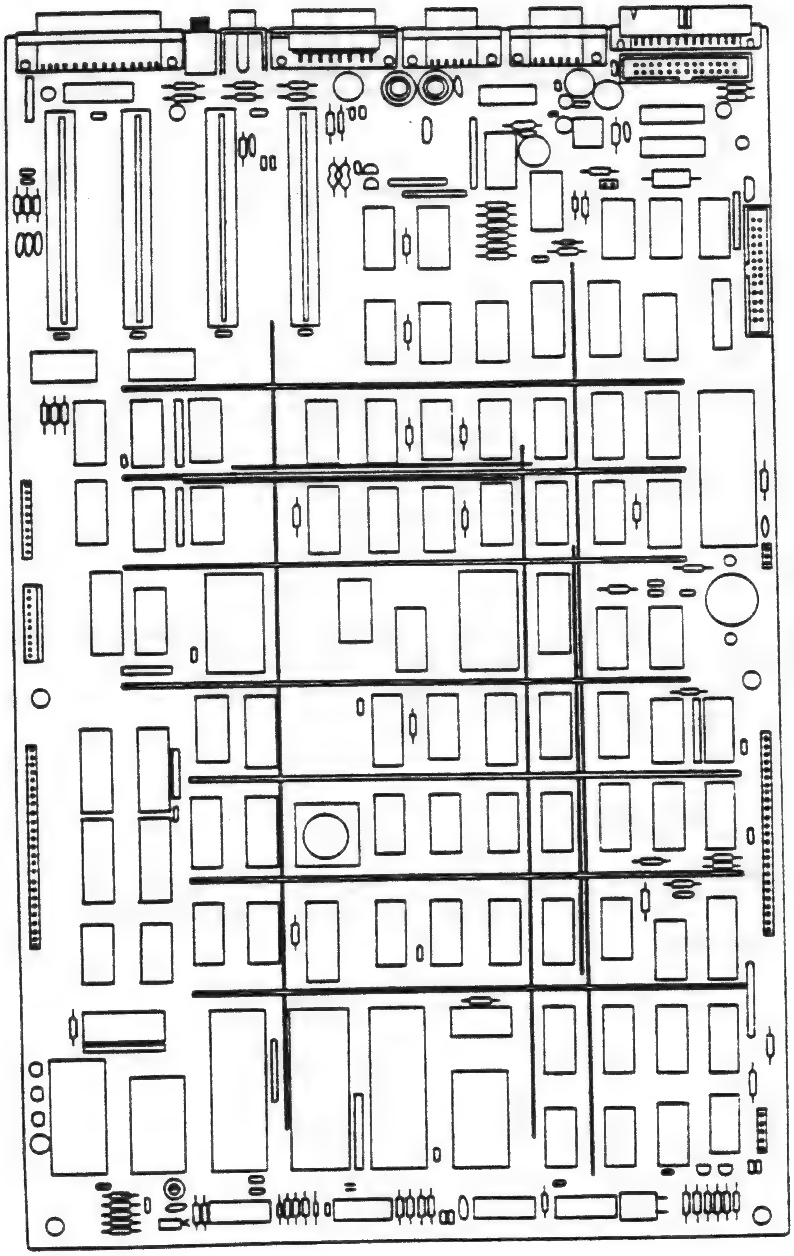
## THE APPLE /// POWER SUPPLY

The power supply, accessible from the bottom of the Apple ///, is housed in the casting. It is a "switching type" power supply that supplies the following voltages:

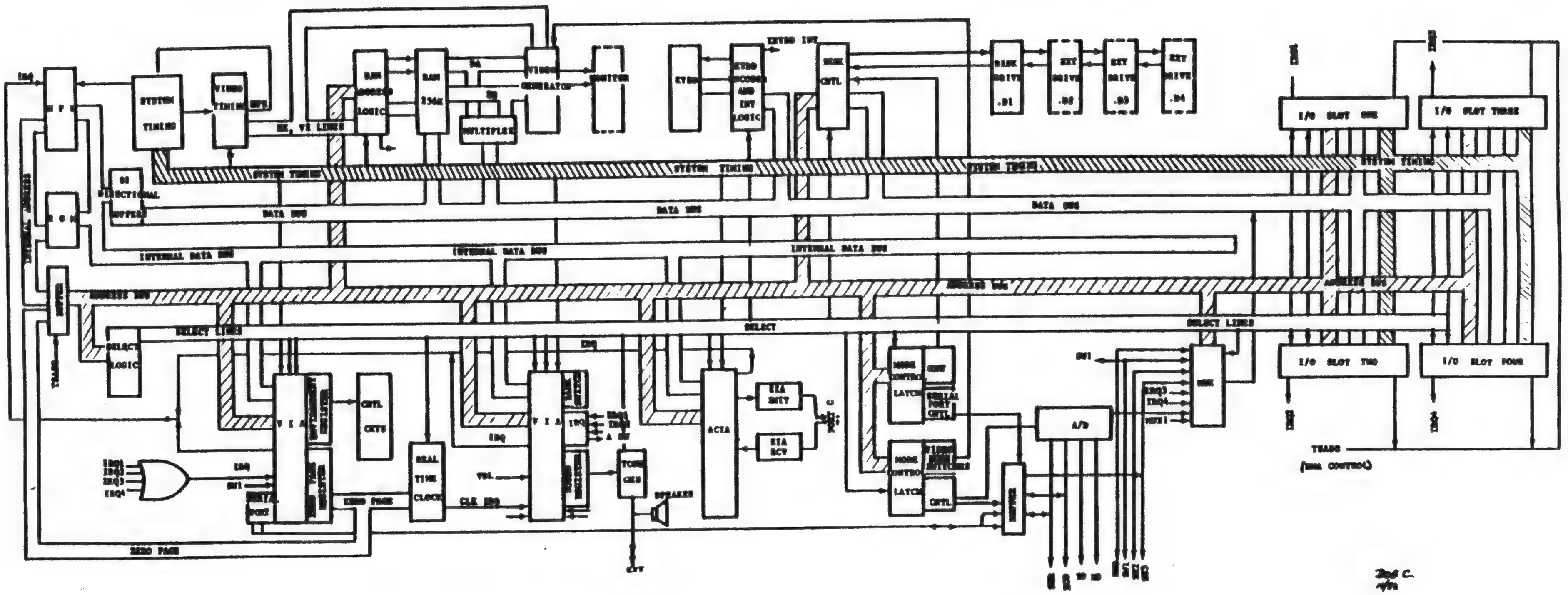
- +5.0 VDC
- +11.8 VDC
- -5.0 VDC
- -12.0 VDC

yet, it consumes less power than a 100 Watt light bulb. The power supply also has several protection features, ie. overvoltage protection.

Now that we have taken a tour of the contents of the Apple /// let us begin to learn the inner workings.



THE APPLE /// MAIN LOGIC BOARD (MODULE)


IRQ
M P U
SYSTEM TIMING
VIDEO TIMING
HE, VE LINES
RAM ADDRESS LOGIC
RAM 256K
MULTIPLEX
VIDEO GENERATOR
MONITOR
KYBD
KYBD ENCODER AND INT LOGIC
KYBD INT
DISK CNTL
DISK DRIVE .D1
EXT DRIVE .D2
EXT DRIVE .D3
EXT DRIVE .D4
I/O SLOT ONE
I/O SLOT THREE
I/O SLOT TWO
I/O SLOT FOUR
SYSTEM TIMING
DATA BUS
INTERNAL DATA BUS
INTERNAL ADDRESS
ADDRESS BUS
SELECT LINES
SELECT
BI DIRECTIONAL BUFFERS
R O M
BUFFER
SELECT LOGIC
IRQ1
IRQ2
IRQ3
IRQ4
IRQ
SW1
SERIAL PORT
V I A
CNTL CKTS
ZERO PAGE
REAL TIME CLOCK
CLK IRQ
VBL
IRQ
A SW
TONE GEN
SPEAKER
ACIA
RIA XMIT
RIA RCV
PORT C
MODE CONTROL LATCH
CONT
SERIAL PORT CNTL
MODE CONTROL LATCH
VIDEO MODE SWITCHES
CNTL
BUFFER
A/D
SW1
IRQ3
IRQ4
MUX1
MUX
TEADS
(DMA CONTROL)
C.

# MEMORY & MEMORY ADDRESSING

## INTRODUCTION TO THE APPLE /// MEMORY

In looking at the Apple /// and its memory we are immediately posed with the problem of how the 6502 processor can handle 128K of RAM, 4K of ROM, and a heavy array of internal and external I/O devices. The Apple /// does indeed do just that, and, further, has the hardware capability of controlling an additional 128K of memory (for a total of 256K).

This "magic" is accomplished by Bank Switching technology. At any one time, the processor can directly address 65K locations. With the addition of the Bank Switch Register, an extended addressing register, the program can call up different banks of 32K RAM space. With other software switches, ROM and all I/O locations can be replaced with RAM. [See Figure 2.1]

The first 8K of memory, from locations 0000 to 1FFF, are fixed. The 32K memory from locations locations 2000 to 9FFF are electrically switchable. The Apple /// can choose any of 15 banks to place in this area at any one time. The maximum amount of storage on the Apple ///, therefore, is equal to 15 Banks x 32K per bank + 32K fixed storage. By comparison, a 128K system would have three banks, a 256K system would have seven, etc.

In addition, the area in the fixed bank from location C000 to CFFF can be switched from RAM memory to I/O space for the slots. The area from F000 to FFFF is also switchable. When the machine is turned on, this area is ROM containing the startup program. This program runs a quick system check then loads SOS in from the internal drive. SOS then switches this area back to RAM.

The extended addressing mode allows any two adjacent banks, N and N+1, to be addressed as a contiguous 64K RAM space. Addresses 0000 to 7FFF are mapped into bank N while addresses 8000 to FFFF are mapped into bank N+1.

The Apple /// has the capability for variable Zero Page locations and Alternate Stack locations. All these features give the Apple /// great flexibility. They also provide means for very large application programs, or applications that need large amounts of RAM space for data crunching.

## SIMPLIFIED MEMORY LOGIC

If we simplify the memory and memory address logic we get three basic elements:

- o the processor
- o the RAM address circuits
- o the RAM array

# Apple /// Memory Map

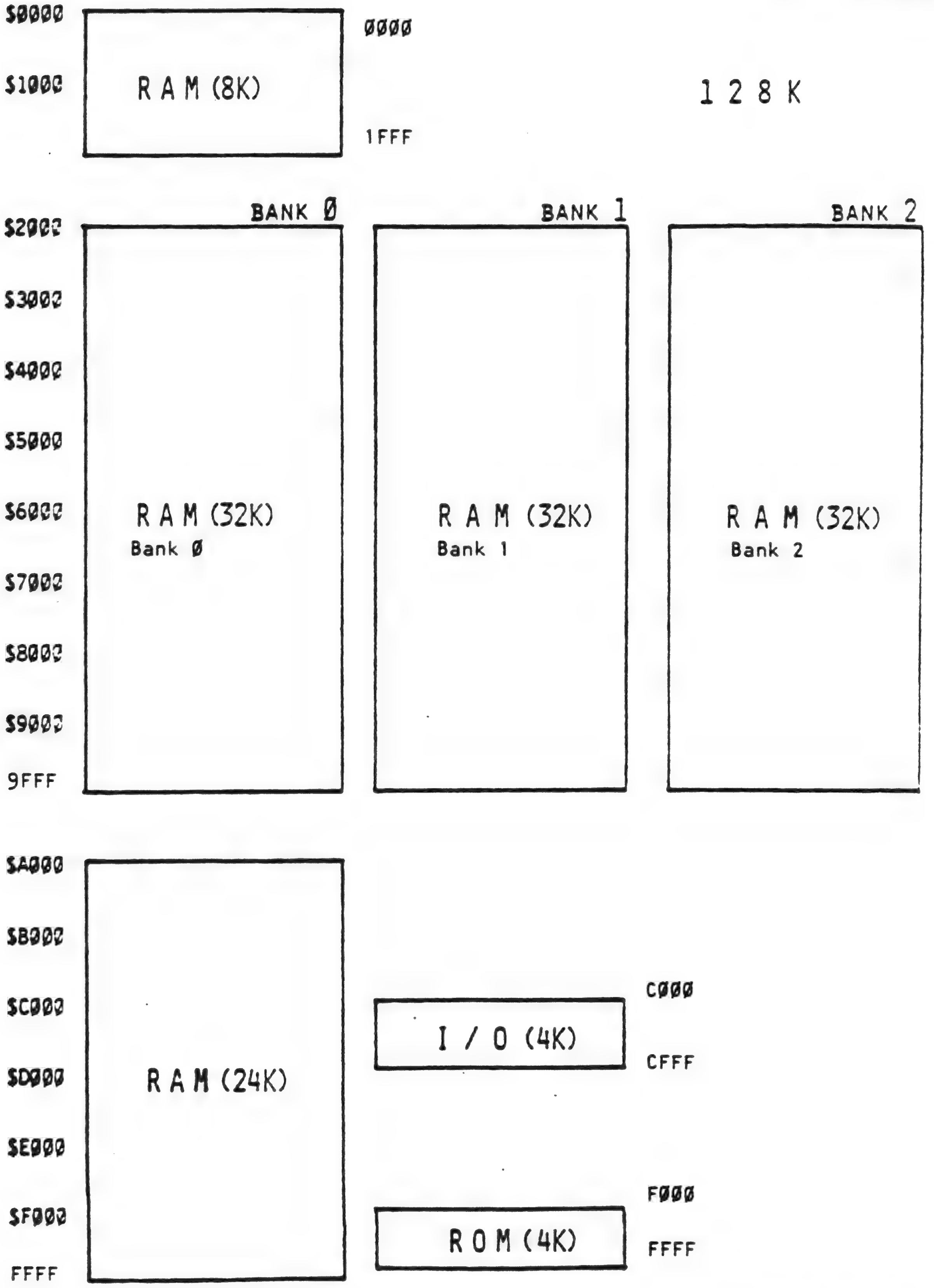

$0000
$1000
RAM (8K)
0000
1FFF
128 K
BANK 0
BANK 1
BANK 2
$2000
$3000
$4000
$5000
$6000
$7000
$8000
$9000
9FFF
RAM (32K)
Bank 0
RAM (32K)
Bank 1
RAM (32K)
Bank 2
$A000
$B000
$C000
$D000
$E000
$F000
FFFF
RAM (24K)
C000
I / O (4K)
CFFF
F000
ROM (4K)
FFFF

**FIG 2.1**

# SIMPLIFIED MEMORY ADDRESS BLOCK DIAGRAM

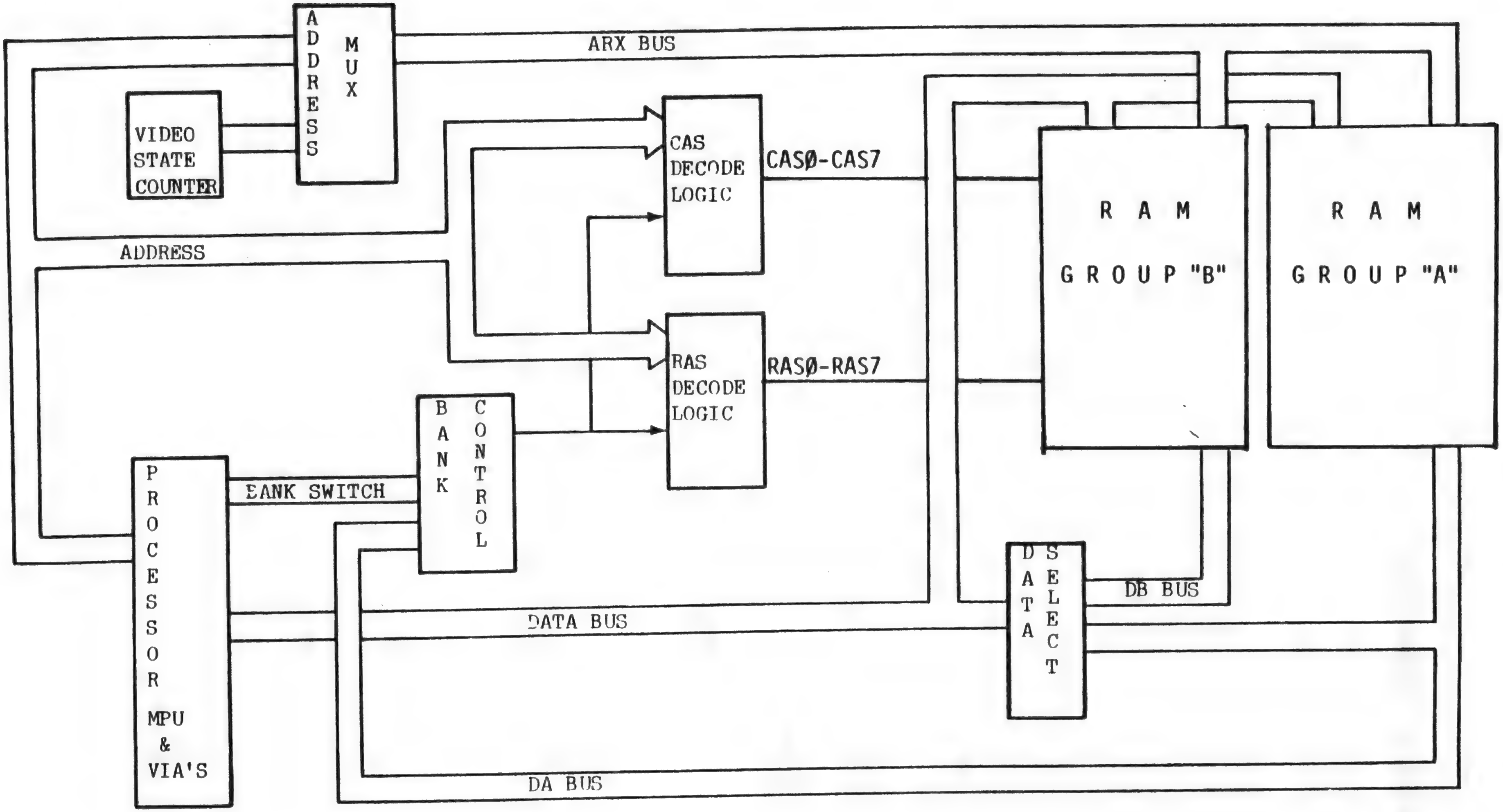

ADDRESS MUX
VIDEO STATE COUNTER
ARX BUS
ADDRESS
CAS DECODE LOGIC
CASØ-CAS7
RAS DECODE LOGIC
RASØ-RAS7
RAM GROUP "B"
RAM GROUP "A"
BANK CONTROL
BANK SWITCH
PROCESSOR MPU & VIA'S
DATA SELECT
DB BUS
DATA BUS
DA BUS

FIG 2.2

In this discussion, the processor is more than just the microprocessor chip; it also contains various external registers and control ROMs which enable the extended addressing and bank switch modes. [Refer to Figure 2.2.]

Very simply, the processor presents an address for memory cycle, which is multiplexed into the address bus, ARX, and is decoded to develop the RAS (Row Address Strobe) and CAS (Column Address Strobe) to the RAM array (RAM group A & B). The direction of the data is controlled by Read/Write*. The selection of which RAM group is being gated to the data bus is controlled by the CAS decode circuits.

The display is memory mapped, the Screen time-shares the RAM on the opposite phase of the processor clock. Both the screen and the processor are running at a 1MHz rate, which means that the RAM is running at a 2MHz rate. One new feature of the Apple /// is that the processor is able to make use of the other "phase" while the screen is off. In other words, any time the screen is off, the processor may run at a full 2MHz rate.

## MEMORY ADDRESSING: BLOCK FLOW

As more detail is added, it is possible to see the basic elements of the complete memory system (For now, we are not considering any to the hardware or I/O).

- In the memory addressing logic of Figure 2.3, the processor now shows the MPU and the two registers for expanded addressing capacity:
  - the bank address register
  - zero page register
- The address circuit is comprised of two sections:
  - the address multiplexer
  - the RAS/CAS decoder
- The RAM array is expanded to show the eight RAMs.

It should be noted that this diagram depicts a 128K system (with a 12V Memory board), and that each of the RAMs shown actually represents eight RAM chips, one for each bit. Each RAM contains 16K bytes. The dotted lines indicate the row of chips that contain the 32K RAM chips. These are actually two 16K RAMs which reside on the one IC package.

## THE PROCESSOR

The MPU is isolated from the rest of the memory by various buffers, muxes, and registers. The mux switches in the Zero Page register whenever the MPU is attempting to reference the zero page.

# BLOCK DIAGRAM MEMORY ADDRESS LOGIC

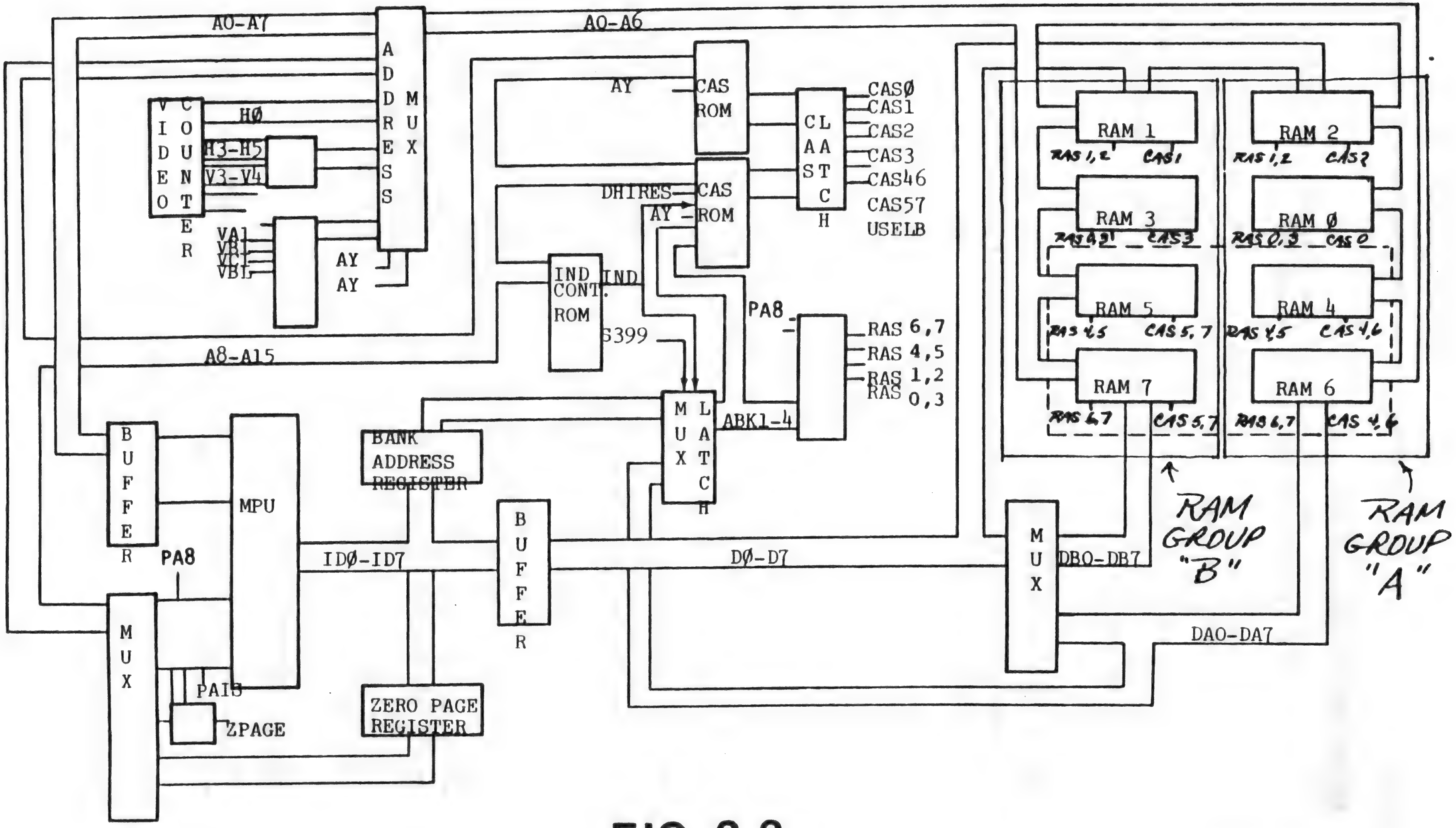

A0-A7
A0-A6
VIDEO COUNTER
H0
H3-H5
V3-V4
VA1
VB1
VC1
VBL
ADDRESS MUX
AY
AY
A8-A15
AY
CAS ROM
DHIRES
AY
CAS ROM
CLASTCH
CAS0
CAS1
CAS2
CAS3
CAS46
CAS57
USELB
IND CONT. ROM
IND
6399
PA8
RAS 6,7
RAS 4,5
RAS 1,2
RAS 0,3
MUX LATCH
ABK1-4
BANK ADDRESS REGISTER
BUFFER
MPU
PA8
MUX
PA15
ZPAGE
ZERO PAGE REGISTER
ID0-ID7
BUFFER
D0-D7
MUX
DB0-DB7
DA0-DA7
RAM 1
RAS 1,2
CAS 1
RAM 3
RAS 0,3
CAS 3
RAM 5
RAS 4,5
CAS 5,7
RAM 7
RAS 6,7
CAS 5,7
RAM 2
RAS 1,2
CAS 2
RAM 0
RAS 0,3
CAS 0
RAM 4
RAS 4,5
CAS 4,6
RAM 6
RAS 6,7
CAS 4,6
RAM GROUP "B"
RAM GROUP "A"

FIG 2.3

- The register may contain the true zero page or may be set to any of 255 other values, under program control.
- The zero page register resides in the VIA and is accessed at FFD0. (On the Main Logic Board this is the VIA at location B6.)
- The Bank Register is located in the other VIA and is accessed at FFEF (at location B5). Zero page selection is independent of bank selection.

## MEMORY ADDRESS MULTIPLEXER

The Memory Address Mux provides the four sets of addresses to the RAM array. They are:

- MPU RAS
- Video RAS
- MPU CAS
- Video CAS

These are time multiplexed by the four states determined by AX* line which is held at a steady state, allowing the processor full access to the RAM.

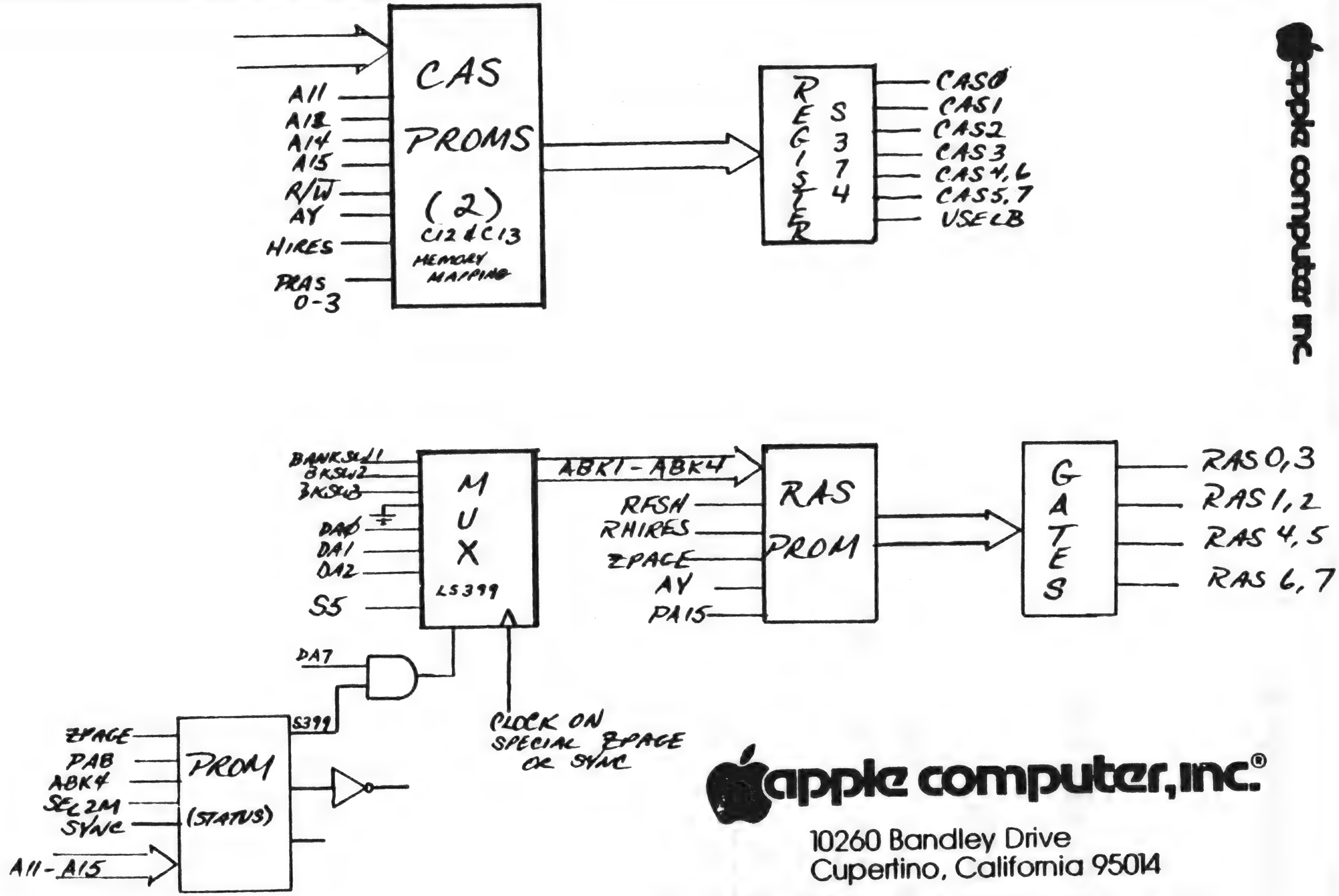
The Video addresses are much the same as in the Apple ][. There is a minor difference in the Summing Circuit, but the technique of condensing undisplayed addresses is the same. There is an additional consideration in the Apple ///, which has a feature requiring additional control of the Video lines. This new feature is called slow scrolling of the screen.

Slow scrolling is accomplished in the Video Mux ROM by the arithmetic offset of the VA, VB, and VC lines. This offset causes characters to be fetched from memory in advance of where the screen actually thinks it is. The character array on the screen shifts up the number of dots determined by the binary weight of the VBX lines. The processor, by monitoring the Vertical Blanking, can then step the VBX lines and scroll the screen by moving in new lines at the bottom, removing the top line, and placing it at the bottom, thus rolling the display.

## RAS/CAS DECODE

The RAS/CAS decode circuit is made from four ROMs, a latch, and a latching mux. The basic inputs to the circuit are:

- the Address Bus
- the Bank Switches
- the Zero Page Select


CAS
PROMS
(2)
C12 & C13
MEMORY MAPPING
A11
A12
A14
A15
R/W
AY
HIRES
PRAS 0-3
REGISTER
S374
CAS0
CAS1
CAS2
CAS3
CAS4,6
CAS5,7
USELB
BANKSW1
BKSW2
BKSW3
DA0
DA1
DA2
S5
MUX
LS399
ABK1 - ABK4
RFSH
RHIRES
ZPAGE
AY
PA15
RAS
PROM
GATES
RAS 0,3
RAS 1,2
RAS 4,5
RAS 6,7
DA7
CLOCK ON SPECIAL ZPAGE OR SYNC
S399
ZPAGE
PAB
ABK4
SEL2M
SYNC
A11-A15
PROM
(STATUS)

apple computer, inc.®
10260 Bandley Drive
Cupertino, California 95014

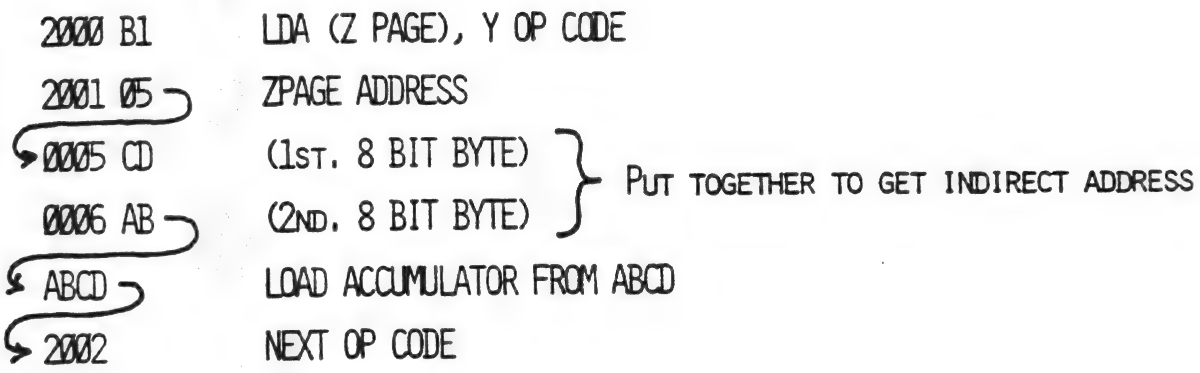
RAS/CAS DECODE LOGIC

BLOCK DIAGRAM

FIG 2.4

INDIRECT ADDRESSING

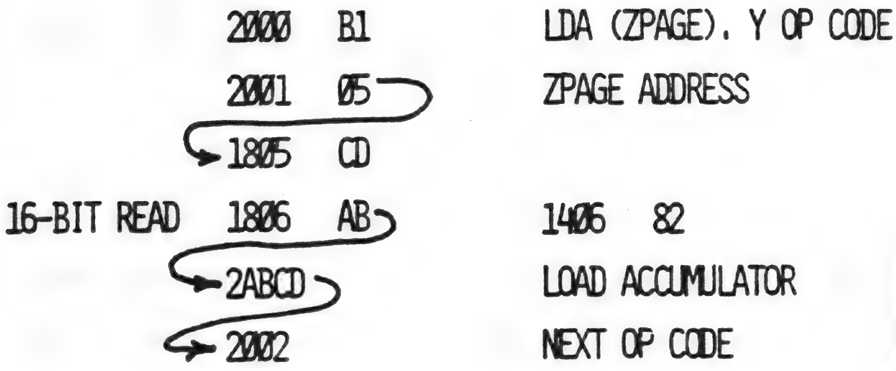
LDA (Z PAGE), Y                    Y REG = 0



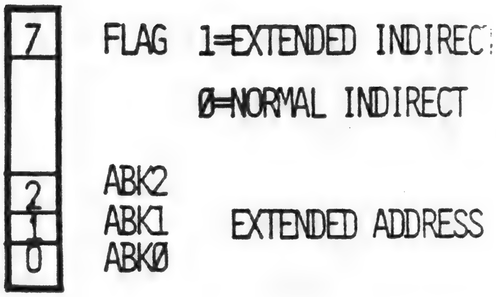
```
2000 B1      LDA (Z PAGE), Y OP CODE
2001 05      ZPAGE ADDRESS
0005 CD      (1ST. 8 BIT BYTE)  }
                                } PUT TOGETHER TO GET INDIRECT ADDRESS
0006 AB      (2ND. 8 BIT BYTE)  }
ABCD         LOAD ACCUMULATOR FROM ABCD
2002         NEXT OP CODE
```

FIG 2.5

IF ZPAGE = 18-1F (IF ZERO PAGE FALLS BETWEEN THE RANGE OF 18-1F)



```
               2000   B1        LDA (ZPAGE). Y OP CODE
               2001   05        ZPAGE ADDRESS
               1805   CD
16-BIT READ    1806   AB        1406   82
               2ABCD            LOAD ACCUMULATOR
               2002             NEXT OP CODE
```


7
FLAG 1=EXTENDED INDIREC
0=NORMAL INDIRECT
2
1
0
ABK2
ABK1
ABK0
EXTENDED ADDRESS

[Refer to Figure 2.4]

Normal or Direct Addressing looks at the address and current bank selection, and enables the appropriate array of 64K RAM. This Direct Addressing always uses RAM 0 and RAM 3. Bank switches determine which of the RAM pairs is used for the other 32K of RAM.

It should be noted that on any read cycle, one RAS line and two CAS lines are selected. In this way, two bytes are always presented to the video circuits and the data selector. During a write cycle only one of each is selected.

The dual byte read usually provides only the information for the new video modes, but there is a new special memory fetch cycle built into the hardware. It is a special extended Indirect Addressing scheme which places the entire memory in virtual access.

By using Indirect Addressing through the zero page containing the 16 bit address, an instruction can address any of the 64K bytes contained in the bank pair. Thus any of the 32K byte RAM banks can be paired with any of their neighbors to form a 64K byte virtual address space.

If, during a zero page reference the zero page register has a value between $18 and $1F ($ means hexadecimal), a special Indirect Mode is called up. This mode looks at the sister fetched data byte on the RAM address bus and also looks at the high order bit. See Figures 2.5 and 2.6.

This special Indirect Mode is determined by the zero page register (X page = Z page EOR $0C) If the bit is zero, the mode is not actualized and the reference continues in a normal manner in the presently selected bank arrangement. But if the High Order Bit (DA7) is high, the bank control mux latch switches to the state determined by the state of the DA0-DA2 lines. This allows the program to have access to another array of special zero pages.

When the system is in this special extended Indirect Mode, the I/O and LSI are totally disabled and the RAM is enabled to the data bus.

## ALTERNATE STACK

Alternate Stack, the new feature of the Apple ///, is not shown in the block diagrams. One of the bits of the Environmental Register (from one of the VIAs) is the Alternate Stack Switch. If the Alternate Stack Switch is selected, the stack associated with that zero page is either the one after the zero page, if the zero page reference is even, or the one previous if the reference is odd (i.e., if zero page is 2B then the stack is located in 2C; if the zero page is 31 then the stack is in 30).

## OTHER BANK SWITCHING

Earlier it was mentioned that the processor can access RAM associated with the addresses that are normally with I/O, ROM, and other circuits. Looking again at the Environmental Register, there are several switches that enable or disable I/O, ROM, and other circuit address decoding. If these switches are selected to disable their associated function, the control ROM, which develops the enable for the RAM data selector, senses the fact that no hardware is being selected and allows RAM data to be read on the bus. No other special enables are needed since RAM is always read for every address presented. It should be noted that a special RAM write enable is used to prevent inadvertant writing into the RAM space associated with the hardware while the hardware is enabled.

## MEMORY & MEMORY ADDRESSING APPENDIX

The attached figures and illustrations are provided for your reference. Little or no explanation has been provided.

This Appendix contains:

- THE APPLE /// MEMORY MAP
- MEMORY MAP SPACE ALLOCATIONS
- ADDRESS LOGIC TRUTH TABLE
- 128K 12V MEMORY BOARD: PHYSICAL MEMORY
- THE 5V MEMORY BOARD: PHYSICAL MEMORY
- ADDRESSING LOGIC EXPRESSIONS
- MPU REGISTERS

# APPLE /// MEMORY MAP

## SOS MEMORY ALLOCATION

| Location | Assignment |
|---|---|
| 0000-1FFF | SOS and Interpreter Workspace |
| 2000-9FFF | Bank 0 Graphics Page 1 and 2 |
| 2000-9FFF | Bank 1 Program |
| 2000-9FFF | Bank 2 Driver and Interprter |
| A000-BFFF | Interpreter |
| C000-CFFF | I/O or SOS Kernal (Bank switchable to RAM) |
| D000-EFFF | SOS Kernal |
| F000-FFFF | Boot ROM OR SOS Kernal |

## ADDRESS ASSIGNMENT

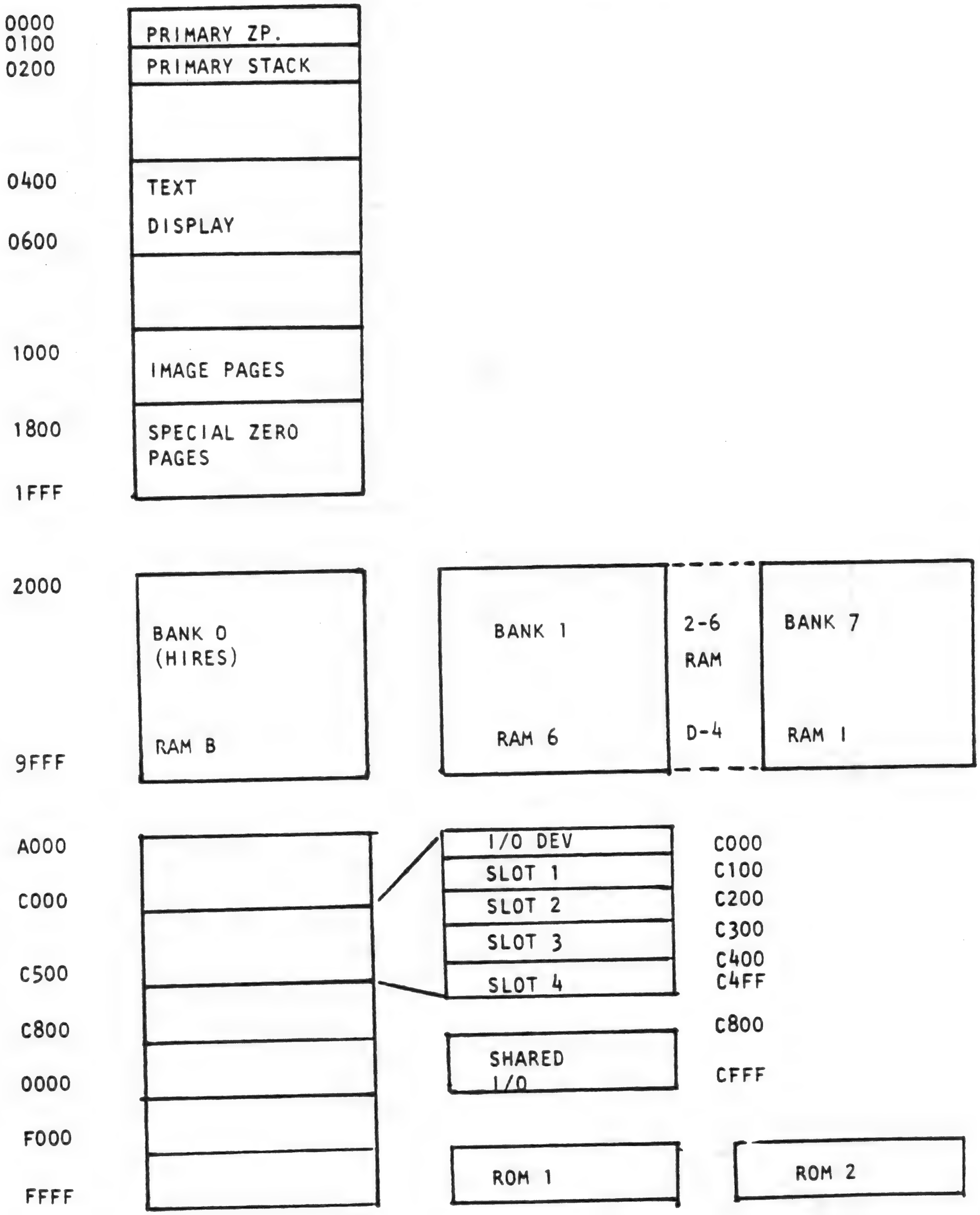
| ADDRESS (HEX) | ASSIGNMENT (FUNCTION) |
|---|---|
| 0000-00FF | Zero Page |
| 0100-01FF | Stack |
| 0200-02FF | Input Buffer |
| 0300-03FF | Open |
| 0400-07FF | Lo-Res Display (Primary) and text |
| 0800-0BFF | Lo-Res Display (Secondary) and text |
| 0C00-0FFF | Open-Reserved for system space |
| 1000-1FFF | Open |
| 2000-3FFF | Hi-Res Pg1 (Primary) switchable to RAM |
| 4000-5FFF | Hi-Res Pg1 (Secondary) switchable to RAM |
| 6000-7FFF | Hi-Res Pg2 (Primary) switchable to RAM |
| 8000-9FFF | Hi-Res Pg2 (Secondary) switchable to RAM |
| A000-BFFF | Open |
| C000-C07F | System I/O |
| C000 | Keyboard "A" bus data |
| C001-C007 | Same as 0000 but not used |
| C008 | Keyboard "B" bus data |
| C009-C00F | Same as C008 but not used |
| C010 | Keyboard reset |
| C011-C02F | Not used in Apple III |
| C030 | Toggle the speaker like in A-11 |
| C031-C03F | Same as C030 but not used |
| C040-C040 | Sound hardware beeper |
| C04E | Character Ram Disable |
| C04F | Character Ram Enable |
| C050 | Clear Text Mode |
| C051 | Set Text Mode |
| C052 | Clear Mix Mode |
| C053 | Set Mix Mode |
| C054 | Clear PG2 Mode |

| | | |
|---|---|---|
| C055 | Set PG2 Mode | |
| C056 | Clear HIRES Mode | |
| C057 | Set HIRES Mode | |
| C058 | Clear EMSOT PDL0 | |
| C059 | SET ENSOT PDL0 | |
| C05A | Clear PDL2 (A/D Addr 2) | |
| C05B | Set PDL2 | |
| C05C | Clear PDLEN (A/D Ramp Start) | |
| C05D | Set PDLEN | |
| C05E | Clear AXC0 (A/D Addr 1) | |
| C05F | Set AXC0 | |
| C060,C068 | Read SW0 | |
| C061,C069 | Read SW1/MGNSW | |
| C062,C06A | Read SW2 | |
| C063,C06B | Read SW3/SC0 | |
| C064,C06C | Read IRQ3 | |
| C065,C06D | Read IRQ4 | |
| C066,C06E | Read PDLOT (A/D Ramp Stop) | |
| C067,C06F | Read MUXI (PRAS Control) | |
| C070 | Access Real Time Clock | |
| C071-C07F | Sames as C070 but not used | |
| C080-COFF | I/O Scot Device Enable | |
| C08F | | |
| C09X | NDevice Select 1 | |
| COAX | NDevice Select 2 | |
| COBX | NDevice Select 3 | |
| COCX | NDevice Select 4 | |
| COD0 | Clear DS A0 | A0,A1=0,0=no select |
| COD1 | Set DS A0 | 1,0=Ena 1 Exit |
| COD2 | Clear DS A1 | 0,1=Ena 2 Exit |
| COD3 | Set DS A1 | 1,1=Ena 3 Exit |
| COD4 | Clear Enable 1 Int | |
| COD5 | Set Enable 1 Int | |
| COD6 | Clear Side 2 | |
| COD7 | Set Side 2 | |
| COD8 | Clear SCR | |
| COD9 | Set SCR | |
| CODA | Clear ENCWRT | |
| CODB | Set ENCWRT | |
| CODC | Clear ENSEL | |
| CODD | Set ENSEL | |
| CODE | Clear ENSIC | |
| CODF | Set ENSIO | |
| COE0 | Clear DPH0 (also VAL) | |
| COE1 | Set DPH0 | |
| COE2 | Clear DPH1 (also VBI) | |
| COE3 | Set DPH1 | |
| COE4 | Clear DPH2 (also VCI) | |
| COE5 | Set DPH2 | |
| COE6 | Clear DPH3 | |
| COE7 | Set DPH3 | |
| COE8 | Disable Motor Drive (strt 2 sec to) COE9 Enable Motor Drive | |
| COEA | Enable Ext | |
| COEB | Enable Int | |

| | |
|---|---|
| COEC | Clear Q6 Note:Q6,Q7 control read |
| COED | Set Q6 write, and sense write |
| COEE | Clear Q7 protect |
| COEF | Set Q7 |
| COF0r | 6551 Rec Data Reg |
| COF0w | 6551 Xmit Data Reg |
| COF1r | 6551 Status Reg |
| COF1w | 6551 Program reset |
| COF2r/w6551 | Command Reg |
| COF3r/w6551 | Control Reg |
| CIXX | NIO Select 1 |
| C100-C7FF | I/O Slot individual ROM Space |
| C100 | Slot 1 Firmware |
| C1FF | |
| C2XX | NIO Select 2 |
| C200-C2FF | Slot 2 Firmware |
| C3XX | NIO Select 3 |
| C300-C3FF | Slot 3 Firmware |
| C3FF | |
| C4XX | NIO Select 4 |
| C400-C4FF | Slot 4 Firmware |
| C500-C7FF | Run Space only |
| C800-CFFF | Expansion Rom Firmware |
| D000-DFFF | Open (system software) |
| E000 | Bank switchable between Rom and Ram |
| FFCX | Always Ram |
| FFDO | Port B VIA-73 "Zero Page Reg" |
| FFD1 | Port A VIA-73 |
| FFD2 | DDR B VIA-73 |
| FFD3 | DDR A VIA-73 |
| FFD4 | Timer 1 low Latch (w)/Counter (r) |
| FFD5 | Timer 1 High Counter |
| FFD6 | Timer 1 Low Latches |
| FFD7 | Timer 1 High Latches |
| FFD8 | Timer 2 Low Latch (w)/Counter (r) |
| FFD9 | Timer 2 High Counter |
| FFDA | Shift Register (serial print) |
| FFDB | Aux Control Reg VIA-73 |
| FFDC | Peripheral Control Register |
| FFDD | Interrupt Flag Register (73) |
| FFDE | Interrupt Enable Register (73) |
| FFDF | ORA/IRA With no handshake |
| FFEO | Port B (97) (sound and slot NMI) |
| FFE1 | Port A (97) Banksw and IRQ's |
| FFE2 | DDR B (97) |
| FFE3 | DDR A (97) |
| FFE4 | Timer 1 Low Latch/Counter |
| FFE5 | Timer 1 High Counter |
| FFE6 | Timer 1 Low Latches |
| FFE7 | Timer 1 High Latches |
| FFE8 | Timer 2 Low Latch/Counter |
| FFE9 | Timer 2 High Counter |
| FFEA | Shift Register (97) |
| FFEB | Aux Control Register (97) |

| | |
|---|---|
| FFEC | Peripheral Control Register (97) |
| FFED | Interrupt Flag Register (97) |
| FFEE | Interrupt Enable Register (97) |
| FFEF | ORA/IRA with no handshake |
| FFE0 | Ram/Rom Bank |
| FFF1 | E/O Bank Switch |
| FFF2 | 2 MHz/MHZ Mode Switch |
| FFF3 | Hires Bank Switch |
| FFF4 | Screen Enable |
| FFF5 | Display Modes |
| FFF6 | Zero Page Register |
| FFF7 | Interrupt Control |
| FFFF | |

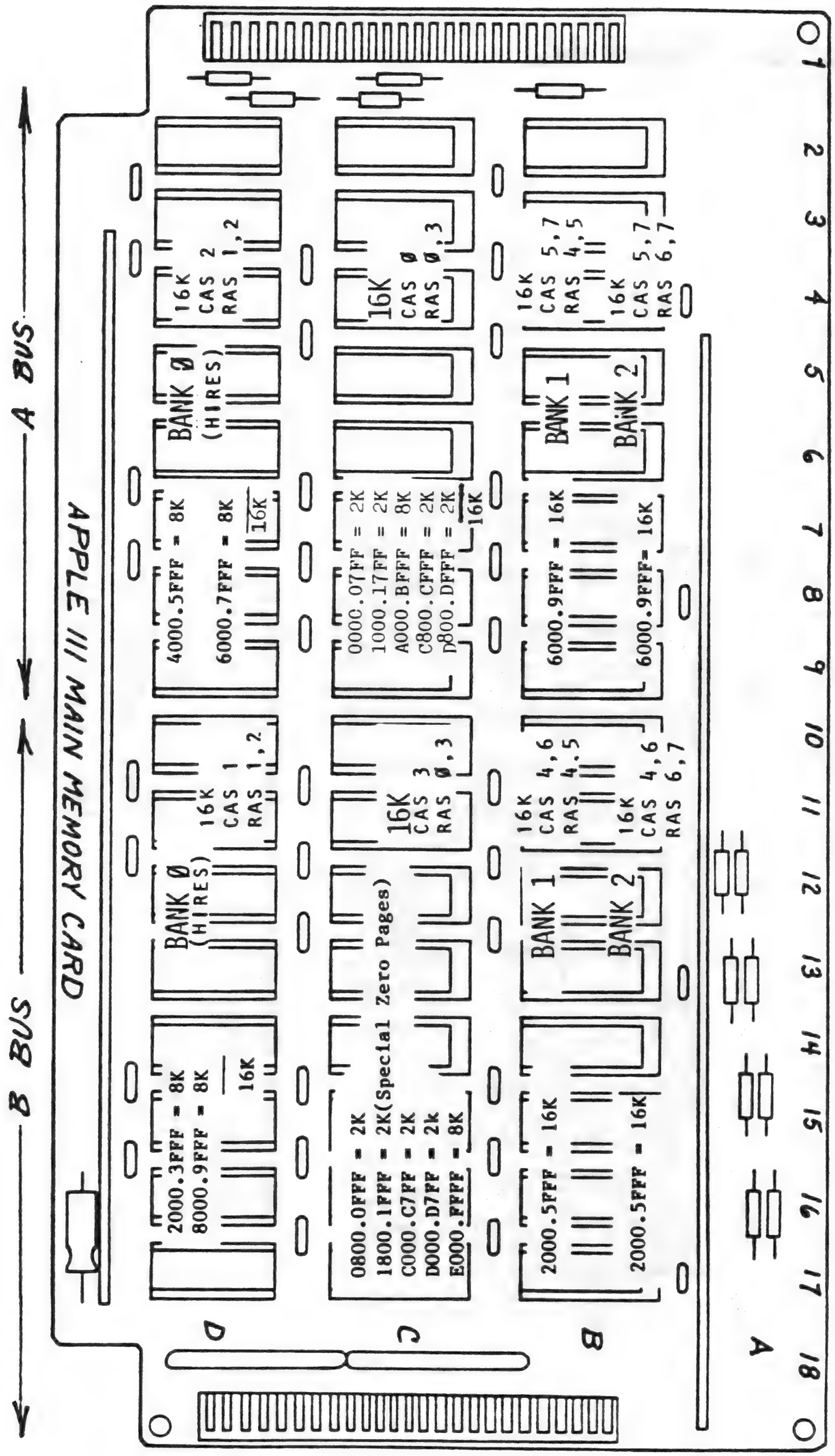
# MEMORY MAP SPACE ALLOCATIONS

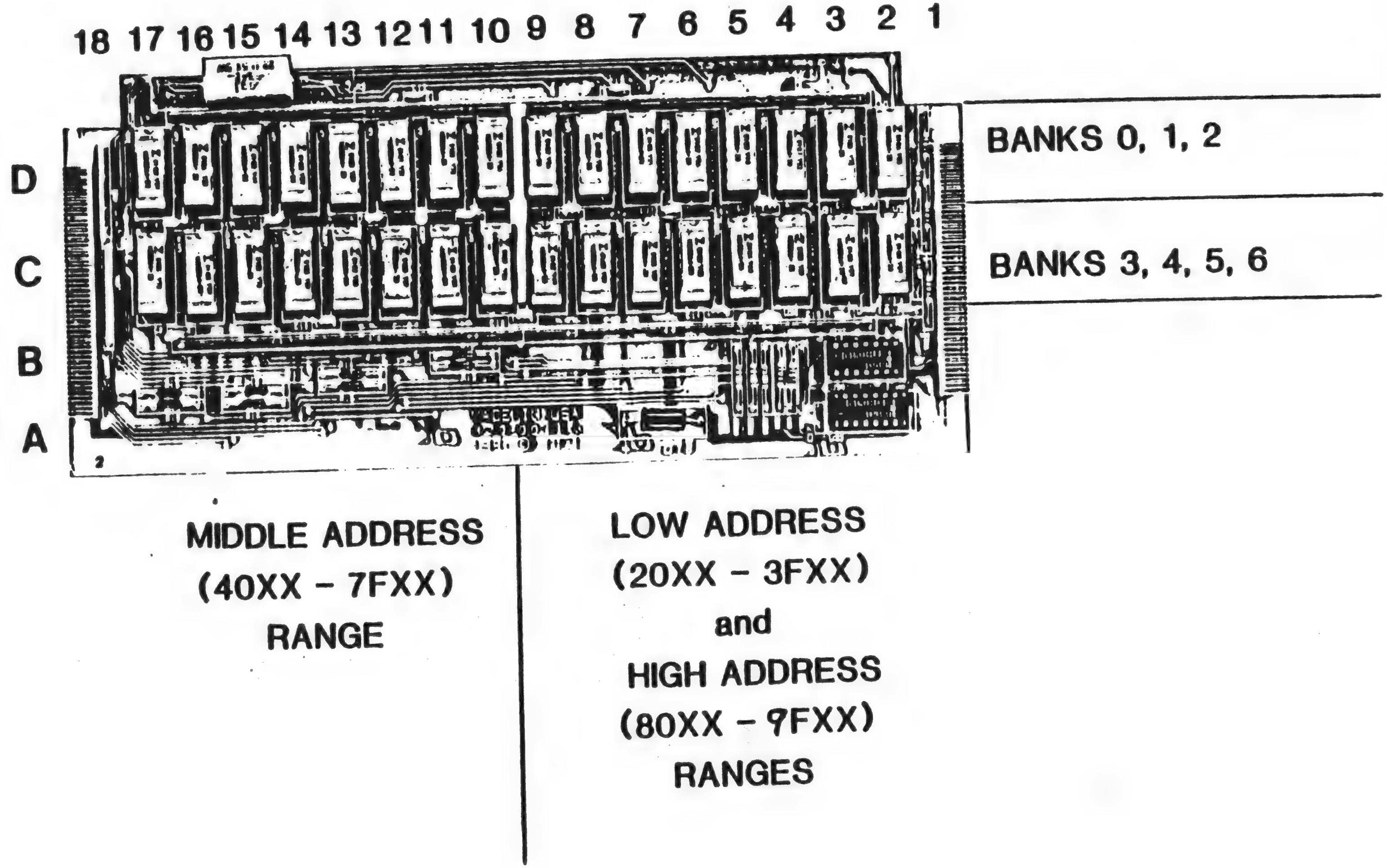

0000
0100
0200
PRIMARY ZP.
PRIMARY STACK
0400
TEXT
DISPLAY
0600
1000
IMAGE PAGES
1800
SPECIAL ZERO
PAGES
1FFF
2000
BANK 0
(HIRES)
RAM B
9FFF
BANK 1
RAM 6
2-6
RAM
D-4
BANK 7
RAM 1
A000
C000
C500
C800
0000
F000
FFFF
I/O DEV
SLOT 1
SLOT 2
SLOT 3
SLOT 4
C000
C100
C200
C300
C400
C4FF
SHARED
I/O
C800
CFFF
ROM 1
ROM 2

** FFCX, FFDX, FFEX ARE ENVIRONMENT ADDRESSES

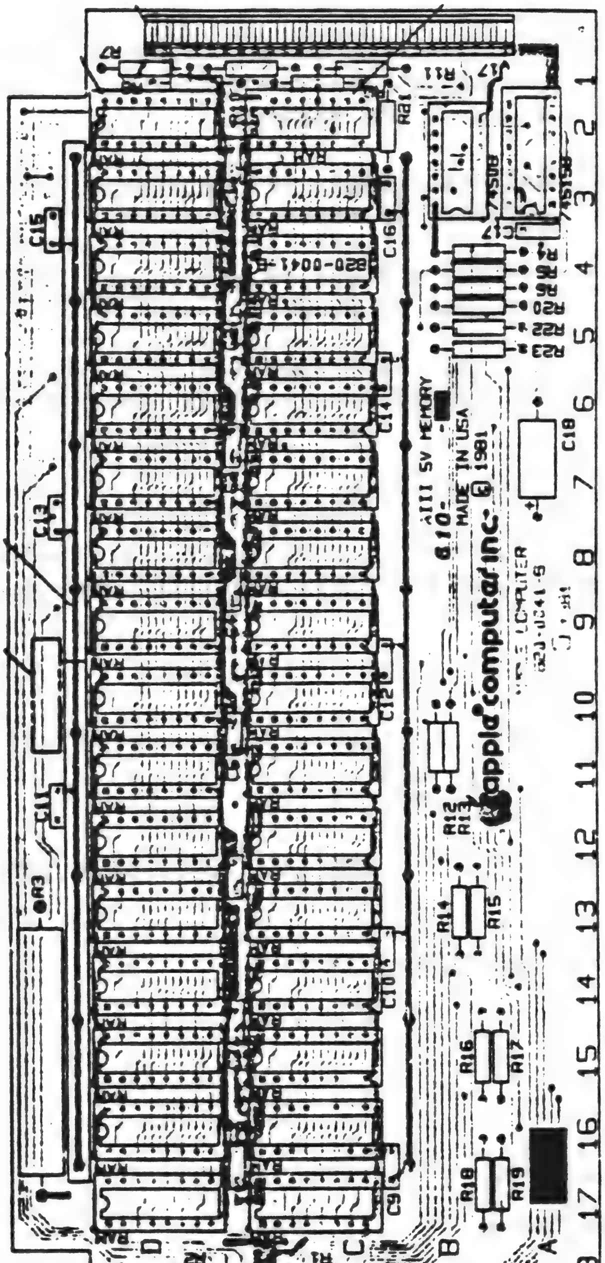
| $\overline{AX}$ | $\overline{AY}$ | AR0 | AR1 | AR2 | AR3 | AR4 | AR5 | AR6 | STATE FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | A0 | A1 | A2 | A3 | A4 | A5 | A7 | MPU GEN RAS ADD. |
| 0 | 1 | H0 | H1 | H2 | Σ1 | Σ2 | Σ3 | V0 | VIDEO GEN RAS ADD |
| 1 | 0 | A6 | A8 | A9 | $A10 \oplus \overline{PCAS0}$ | $A11 \oplus \overline{PCAS0}$ | A12 | $PCAS1 \oplus (A15 \oplus \overline{PCAS0,3})$ | MPU GEN CAS ADD |
| 1 | 1 | Σ4 | V1 | V2·V5 | MUX1 | MUX2 | MUX3 | $\overline{PG2}$ | VIDEO GEN CAS ADD |

ADDRESS LOGIC TRUTH TABLE


APPLE III MAIN MEMORY CARD
A BUS
B BUS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
A
B
C
D
16K CAS 2 RAS 1,2
BANK Ø (HIRES)
4000.5FFF = 8K
6000.7FFF = 8K
16K
16K CAS 1 RAS 1,2
BANK Ø (HIRES)
2000.3FFF = 8K
8000.9FFF = 8K
16K
16K CAS Ø RAS Ø,3
0000.07FF = 2K
1000.17FF = 2K
A000.BFFF = 8K
C800.CFFF = 2K
D800.DFFF = 2K
16K
16K CAS 3 RAS Ø,3
(Special Zero Pages)
0800.0FFF = 2K
1800.1FFF = 2K
C000.C7FF = 2K
D000.D7FF = 2k
E000.FFFF = 8K
16K CAS 5,7 RAS 4,5
16K CAS 5,7 RAS 6,7
BANK 1
BANK 2
6000.9FFF = 16K
6000.9FFF= 16K
16K CAS 4,6 RAS 4,5
16K CAS 4,6 RAS 6,7
BANK 1
BANK 2
2000.5FFF = 16K
2000.5FFF = 16K


18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
D
C
B
A
BANKS 0, 1, 2
BANKS 3, 4, 5, 6
MIDDLE ADDRESS
(40XX – 7FXX)
RANGE
LOW ADDRESS
(20XX – 3FXX)
and
HIGH ADDRESS
(80XX – 9FXX)
RANGES

# THE 5V MEMORY BOARD ( 256K )


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
A
B
C
D
R1
R2
R3
R11
R21
R4
R5
R6
R20
R22
R23
R12
R13
R14
R15
R16
R17
R18
R19
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
J17
J18
74S08
74S158
820-0041-B
AIII 5V MEMORY
MADE IN USA
© 1981
apple computer inc.

## HOW TO READ PROM (ROM) LOGIC EXPRESSIONS

X′ -- The single quote at the end of an expression means that the state of the signal is true when low, or it may represent the inversion of the state of the signal.

* -- Defines a logic AND operation. The expressions on either side of the asterisk is ANDed.

+ -- Defines a logic OR operation. The expression on either side of the asterisk is OR′d.

() -- Defines the boundaries of a logic expression. A new expression is defined by what ever is inside of the brackets.

### RULES FOR INTERPRETATION

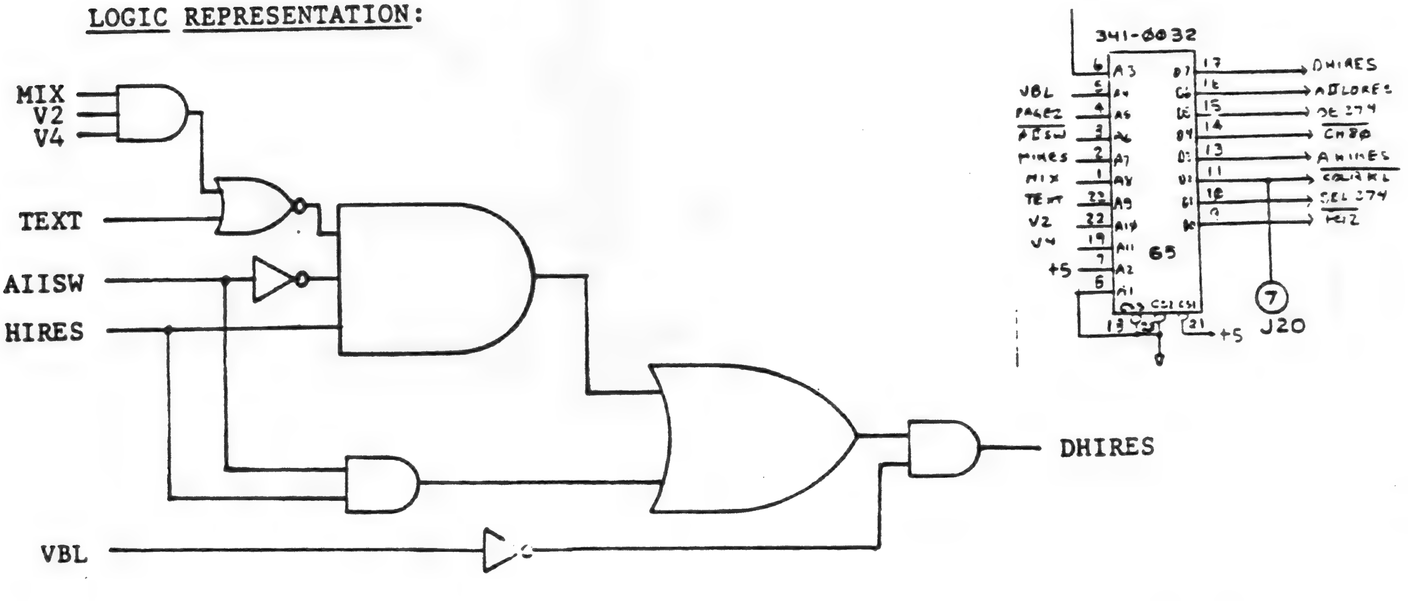
1. Always interpret (transform) the expression within the brackets first.
2. Interpret AND (*) logic operations before OR (+) operations.

EXAMPLE:

| Given: | INPUTS: | AIISW′ | HIRES | TEXT |
|---|---|---|---|---|
| | | MIX | V2 | V4 |
| | | VBL | | |

OUTPUT: DHIRES = (AIISW*HIRES*(TEXT+MIX*V2*V4)′+AIISW′*HIRES)*VBL′

LOGIC REPRESENTATION:


MIX
V2
V4
TEXT
AIISW
HIRES
VBL
DHIRES
341-0032
VBL
PAGE2
AIISW
HIRES
MIX
TEXT
V2
V4
+5
A3
A1
A2
65
DHIRES
A LORES
SEL 274
CH80
A HIRES
SEL 274
+5
7
J20

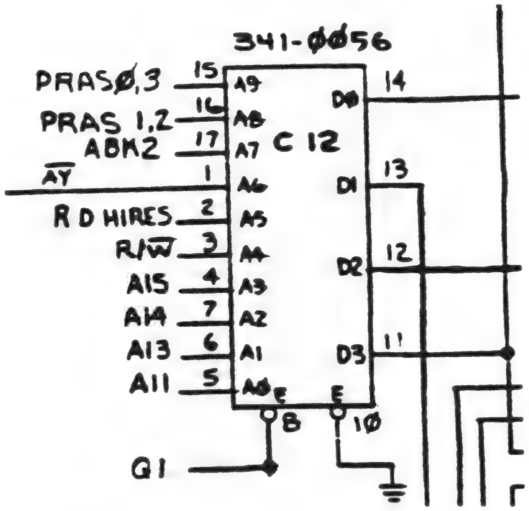
A=A11
B=A13
C=A14
D=A15
E=R/WN
F=DHIRES
G=AY’
H=ABK2
I=PRAS1,2
J=PRAS0,3
D0=PCAS0’
D1=PUSELB
D2=PCAS3
D3=PCAS3’

PCAS0’=(PRAS0, 3 * (DHIRES’ *AY’ +AY* (A15’* A14’ * A13’ *A11’ *R/WN’ + A15’ *A14’ *A13’* R/WN+A15*A14’*A13’ *A11)))’

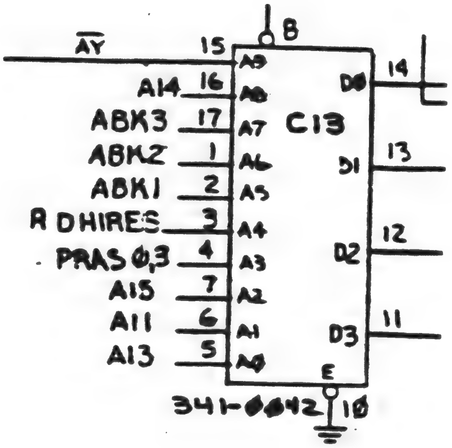
PUSELB=PRAS0, 3 * (A15’ *A14’ *A13’ *A11 +A15 *A14 *A13’ *A11’ +A15 *A14 *A13) +PRAS0, 3 *PRAS1, 2 *(A15’ *A14’ *A13+A15* A14’ *A13’) +PRAS0, 3 *PRAS1,2 ’*(A15’ *A14’ *A13+A15’ *A14 *A13’) +PRAS0, 3 ’* PRAS1, 2 * (A14’ *A13’ +A14 *A13) +PRAS0, 3 ’ *PRAS1, 2 ’ *A14’

PCAS3=PRAS0, 3 * (DHIRES ’ *AY ’ + AY* (A15’ *A14’ *A13’ *A11 + A15 *A14 A13’ *A11’ +A15 *A14 *A13))

PCAS3’=(PRAS0,3 * (DHIRES ’ *AY’ +AY* (A15’ *A14’ *A13’ *A11+A15 *A14 *A13’ *A11’ +A15* A14* A13)))’

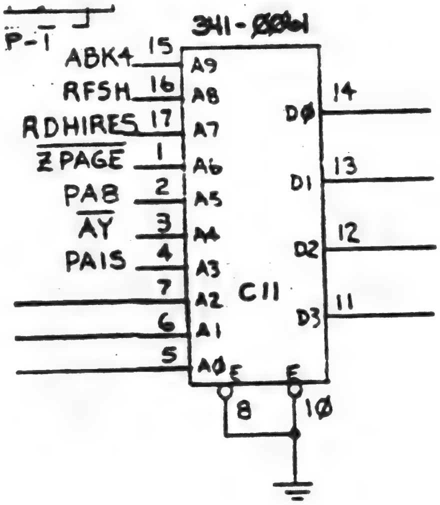

341-0056
PRAS0,3
PRAS 1,2
ABK2
$\overline{AY}$
R D HIRES
R/$\overline{W}$
A15
A14
A13
A11
Q1
15
16
17
1
2
3
4
7
6
5
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
C 12
D0
D1
D2
D3
14
13
12
11
E
E
B
10

```
A=A13
B=A11
C=A15
D=PRASO,3
E=DHIRES
F=ABK1
G=ABK2
H=ABK3
I=A14
J=AY'
D0=PCAS4,7'
D1=PCAS5,6'
D2=PCAS1'
D3=PCAS2

PCAS4,7'= (AY*PRASO, 3 * (ABK1*ABK2*ABK3'+ABK3* (ABK1' + ABK2'))* (A15'
          *A14) +AY* PRASO,3 '* (ABK1' *ABK2*ABK3'*A14+ABK1*ABK2*ABK3'+ABK2'
          *ABK3+ABK1' *ABK2*ABK3*A15') *(A14' *A13+A14*A13))'

PCAS5,6'= (AY8PRASO,3 *(ABK1*ABK2*ABK3' +ABK3* (ABK1' +ABK2'))* (A15'*A14'
          *A13+A15*A14' *A14'*A13') +AY*PRASO, /3 '*(ABK1'*ABK2*ABK3' *A15+
          ABK1*ABK2*ABK3*'+ABK2'*ABK3+ABK1'*ABK2*ABK3*A15') *(A14'*A13'A14*
          A13))'

PCAS1' = (DHIRES *AY'+AY*PRASO, 3 * (ABK3' * (ABK1'+ABK2') +ABK1*ABK2*ABK3)
        * (A15'* A14' *A13+A15*A14' *A13') +AY*PRASO, 3 '*(ABK2' *ABK3'+ABK1'
        *ABK2*ABK3'*A15') * (A14'* A13'+A14*A13))'

PCAS2' = (DHIRES *AY' +AY*PRASO,3 *(ABK3'* (ABK1' +ABK2') +ABK1*ABK2*ABK3)
        *A15'* A14+AY*PRASO,3 '*(ABK2'*ABK3'+ABK1'*ABK2*ABK3'*A15) *(A14'
        *A13+A14*A13'))'
```

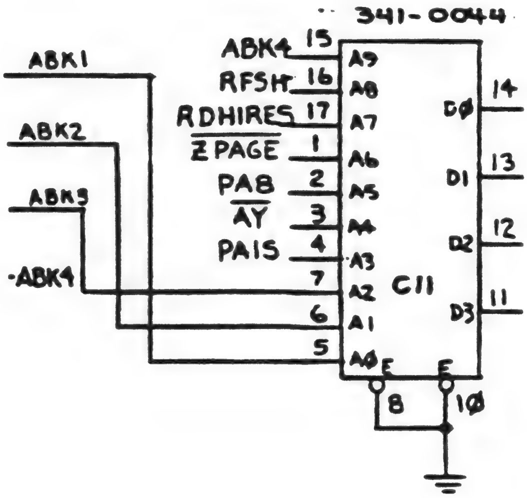


AY
15
8
A9
14
A14
16
A8
D0
ABK3
17
A7
C13
ABK2
1
A6
D1
13
ABK1
2
A5
R DHIRES
3
A4
12
PRAS 0,3
4
A3
D2
A15
7
A2
A11
6
A1
D3
11
A13
5
A0
E
341-0042
10

```
RAS 258

A=ABK1
B=ABK2
C=ABK3
D=PA15
E=AY'
F=PA8
G=ZPAGE'
H=DHIRES
I=RFSH
J=ABK4
D0=PRAS0,3
D1=PRAS1,2
D2=PRAS4,5
D3=PRAS6,7

PRAS0,3 = AY'* (DHIRES' +RFSH) + ((ABK4* (ZPAGE*PA8')')'+ABK4* (ZPAGE*PA8)'
        '*ABK1* ABK2*ABK3)*AY PRAS1,2=AY'+AY PRAS4,5=AY'+AY*(ABK4* (ZPAGE*
        PA8')')'*(ABK1*ABK2*ABK3'+ABK1'*ABK2*ABK3' *PA15+ABK1'* ABK2'*PA15'
        +ABK1*ABK2*ABK3)  PRAS6,7 +AY'*DHIRES'+AY* (ABK4*(ZPAGE*PA8')')'*
        (ABK1* (ABK2' +ABK3')) +AY*ABK4* (ZPAGE*PA8')'* (PA15'*ABK1* (ABK2'
        +ABK3') +PA15*ABK1'* (AKB2' + ABK3'))
```


P-1
341-0061
ABK4 15 A9
RFSH 16 A8
RDHIRES 17 A7
ZPAGE 1 A6
PA8 2 A5
AY 3 A4
PA15 4 A3
7 A2
6 A1
5 A0
C11
E E
8 10
D0 14
D1 13
D2 12
D3 11

```
RAS.2.TEXT

A-ABK1
B=ABK2
C=ABK3
D=PA14 5
E-AY'
F=PA8
G=ZPAGE
H=DHIRES
I=RFSH
J=ABK4
D0=PRAS0,3
D1-PRAS1,2
D2=PRAS4,5
D3=PRAS6,7

PRAS0, 3 =AY'* (DHIRES'+RFSH) + ((ABK4* (ZPAGE*PA8')') ' +ABK1*ABK2*ABK3)
         *AY

PRAS1,2  =AY'* (DHIRES+RFSH) =AY* (ABK1'* AKB2'*ABK3'* (ABK4* (ZPAGE*PA8')
         '**PA15)'+ABK1*ABK2*ABK3) +AY*ABK3'* (ABK1'* ABK2* ABK4* (ZPAGE*
         PA8') '*PA15+ABK1*ABK2*(ABK4* (ZPAGE*PA8') *PA15)')

PRAS4,5 =RFSH*AY'+AY*ABK2'*ABK3'* (ABK1'*ABK4* (ZPAGE*PA8') 'PA15+ABK1*
        (ABK4* (ZPAGE*PA8') '*PA15)')

PRAS6,7 =RFSH*AY'+AY*ABK3'* (ABK1*?BK2'*ABK4* (ZPAGE*PA8') '*PA15+ABK1'*
        ABK2* (ABK4* (ZPAGE*PA8') '*PA15)')
```

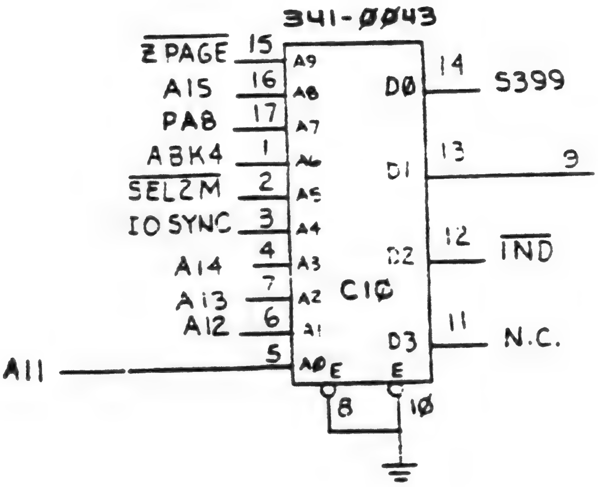

341-0044
ABK1
ABK2
ABK3
ABK4
ABK4
RFSH
RDHIRES
ZPAGE
PA8
AY
PA15
15
16
17
1
2
3
4
7
6
5
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
C11
D0
D1
D2
D3
14
13
12
11
E
E
8
10

A=A11
B=A12
C=A13
D=A14
E=IOSYNC
F=SEL2M'
G=ABK4
H=PA8
I=15
K=PAGE'
D0=S399
D1=PRDY'
D2=IND'

S399=ZPAGE*PA8' *A15' *A14' *A13' *A12* A11

PRDY'=IOSYNC *SEL2M *ABK4

IND'= (ABK4* (ZPAGE* PA8') ')'


341-0043
$\overline{\text{Z PAGE}}$
15
A9
A15
16
A8
PA8
17
A7
ABK4
1
A6
$\overline{\text{SEL2M}}$
2
A5
IO SYNC
3
A4
A14
4
A3
A13
7
A2
A12
6
A1
A11
5
A0
E
E
8
10
C10
D0
14
S399
D1
13
9
D2
12
$\overline{\text{IND}}$
D3
11
N.C.

U175 1. TEXT

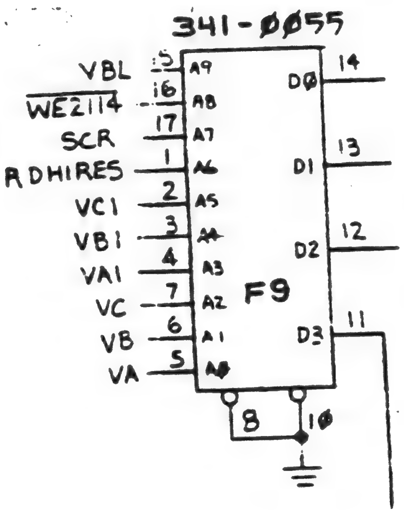
A=VA
B=VB
C=VC
D=VA1
E=VB1
F=VC1
G=DHIRES
H=SCR
I=WE2114'
J=VBL
DO=MUX1
D1=MUX2
D2=MUX3
D3=ENHREG'

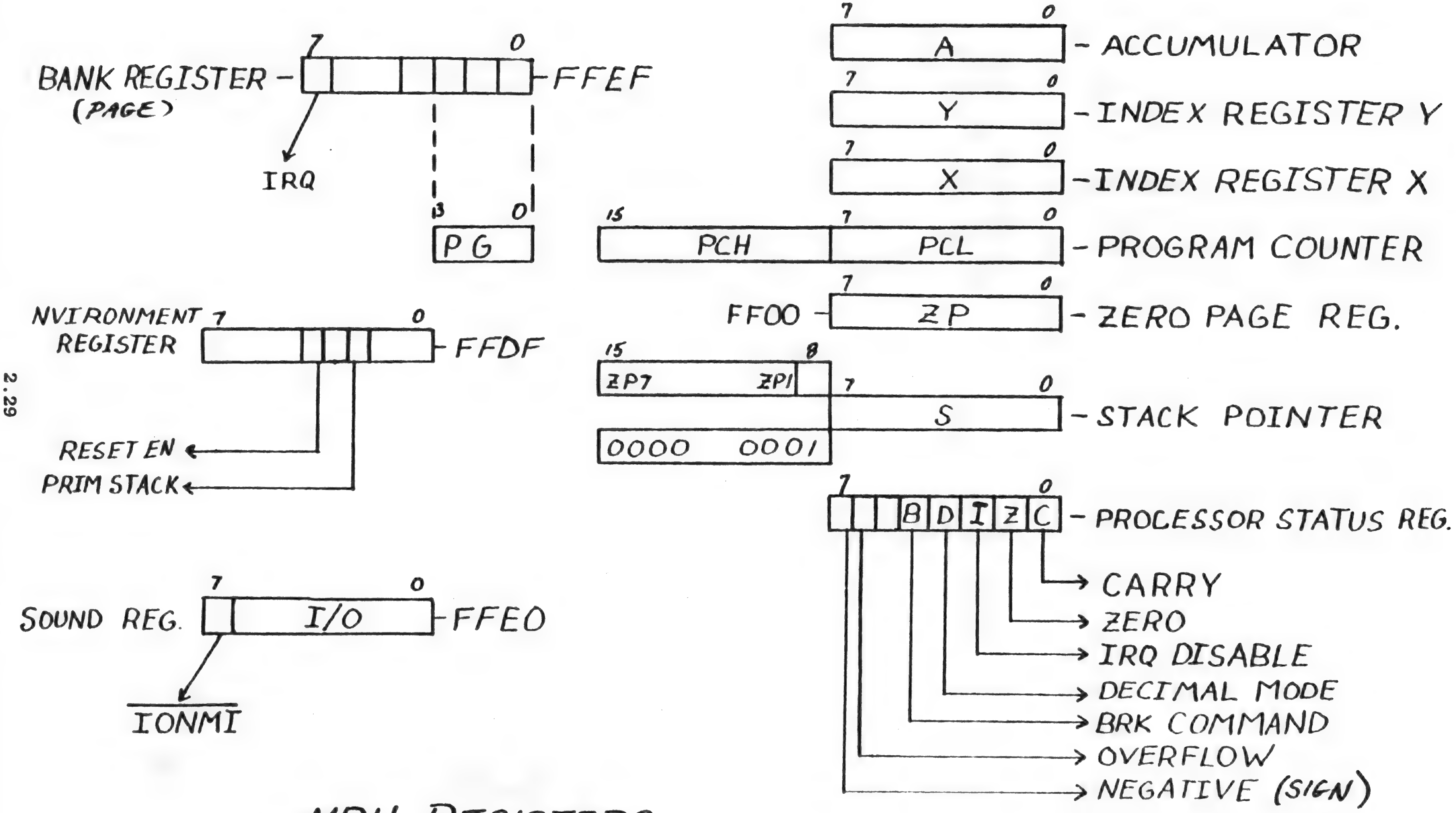
MUX1=(DHIRES' +SCR * (VA* VA1' +VA' *VA1) + SCR' *VA) * (VBL' + WE2114)
+VBL * WE2114'

MUX2=DHIRES* (SCR* (VA* VA1* (VB* VB1' +VB'* VB1)'+ (VA* VA1)'* (VB* VB1'
+VB * VB1) ) +VB* SCR')

MUX3=DHIRES * (SCR* ((VA* VA1* (VB+ VB1) +VB* VB1) * (VC* VC1'+VC'* VC1)
'+(VA* VA1* (VB+ VB1) +VB * VB1) '*(VC * VC1) ) +VC* SCR')

ENHREG'=DHIRES' *WE2114'


341-0055
VBL
$\overline{\text{WE2114}}$
SCR
R DHIRES
VC1
VB1
VA1
VC
VB
VA
15
16
17
1
2
3
4
7
6
5
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
F9
D0
D1
D2
D3
14
13
12
11
8
10


BANK REGISTER
(PAGE)
7
0
FFEF
IRQ
3
0
P G
NVIRONMENT REGISTER
7
0
FFDF
RESET EN
PRIM STACK
SOUND REG.
7
0
I/O
FFE0
IONMI
7
0
A
ACCUMULATOR
Y
INDEX REGISTER Y
X
INDEX REGISTER X
15
PCH
PCL
PROGRAM COUNTER
FF00
ZP
ZERO PAGE REG.
8
ZP7
ZP1
S
STACK POINTER
0000
0001
B
D
I
Z
C
PROCESSOR STATUS REG.
CARRY
ZERO
IRQ DISABLE
DECIMAL MODE
BRK COMMAND
OVERFLOW
NEGATIVE (SIGN)

MPU REGISTERS

## I/O DEVICE STROBES

| | |
|---|---|
| 0X | KEYBOARD READ |
| 1X | RESET KEYBAORD |
| 2X | N.C . |
| 3X | Speake Toggle |
| 4X | Beeper |
| 5X | Display Regiater |
| 6X | Switch Register |
| 7X | Real Time Clock |
| 8X | N.C. |
| 9X | |
| AX | Slot 1-4 |
| BX | DEVSEL |
| CX | |
| DX | I/O CONTROL REGISTER |
| EX | DISK REGISTER |
| FX | ACIA |

COXX

## KEYBOARD DATA

| | |
|---|---|
| 0 | ASCII0 |
| 1 | ASCII1 |
| 2 | ASCII2 |
| 3 | ASCII3 |
| 4 | ASCII4 |
| 5 | ASCII5 |
| 6 | ASCII6 |
| 7 | KBO FLAG |

C000

## KEYBOARD STATUS

| | |
|---|---|
| 0 | ANY KEY DOWN |
| 1 | SHIFT |
| 2 | CONTROL |
| 3 | CAPSLOCK |
| 4 | APPLE I |
| 5 | APPLE II |
| 6 | KEYBOARD PRESENT |
| 7 | ASCII7 |

C008

## VIA

| | | |
|---|---|---|
| CA1 | SLOT INT. | |
| CA2 | SWI/MARGIN INT. | |
| CB1 | SERVICE CLOCK | SILENTYPE |
| CB2 | SERVICE DATE/PDLO | |

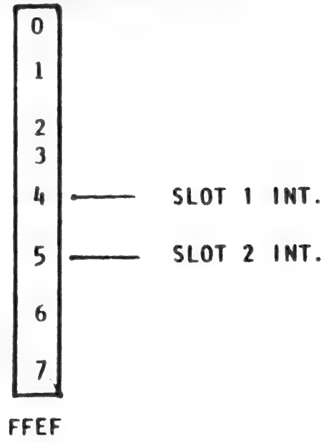
FFDX

## VIA

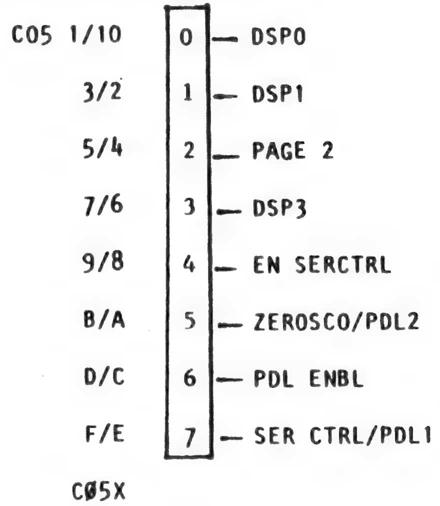
| | |
|---|---|
| CA1 | RT CLOCK INT. |
| CA2 | KEYBOARD UNIT |
| CB1 | VERTICAL BLANKING |
| CB2 | VERTICAL BLANKING |

FFEX

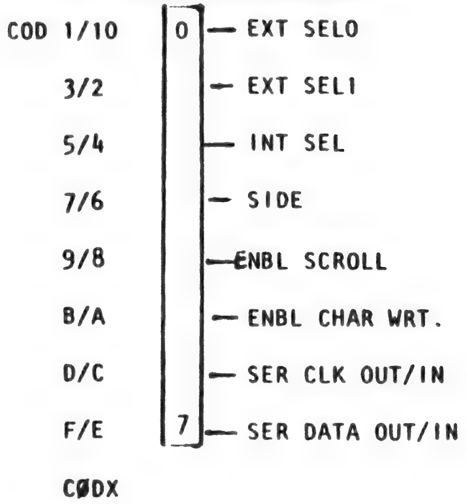
## BANK PAGE REGISTER


0
1
2
3
4 — SLOT 1 INT.
5 — SLOT 2 INT.
6
7
FFEF

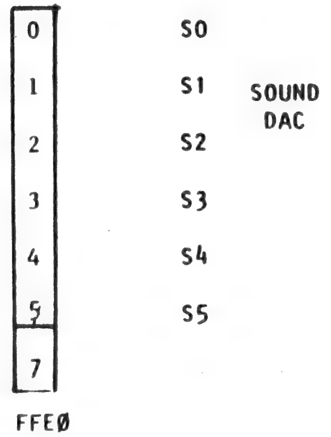
## DISPLAY REGISTER


C05 1/10 0 — DSP0
3/2 1 — DSP1
5/4 2 — PAGE 2
7/6 3 — DSP3
9/8 4 — EN SERCTRL
B/A 5 — ZEROSCO/PDL2
D/C 6 — PDL ENBL
F/E 7 — SER CTRL/PDL1
C05X

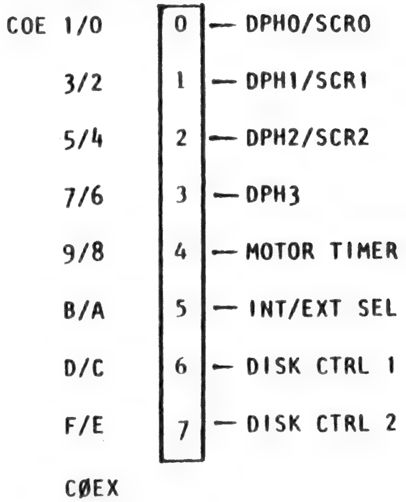
## I/O CONTROL REGISTER


C0D 1/10 0 — EXT SEL0
3/2 — EXT SEL1
5/4 — INT SEL
7/6 — SIDE
9/8 — ENBL SCROLL
B/A — ENBL CHAR WRT.
D/C — SER CLK OUT/IN
F/E 7 — SER DATA OUT/IN
C0DX

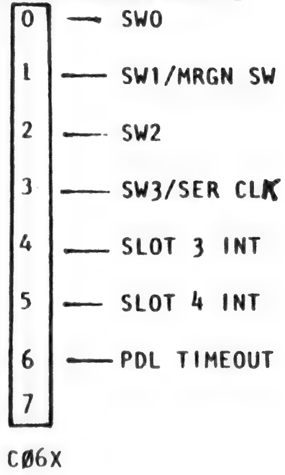
## SOUND REGISTER


0 S0
1 S1
2 S2
3 S3
4 S4
5 S5
7
SOUND DAC
FFE0

## DISK REGISTER


C0E 1/0 0 — DPH0/SCR0
3/2 1 — DPH1/SCR1
5/4 2 — DPH2/SCR2
7/6 3 — DPH3
9/8 4 — MOTOR TIMER
B/A 5 — INT/EXT SEL
D/C 6 — DISK CTRL 1
F/E 7 — DISK CTRL 2
C0EX

## SWITCH REGISTER


0 — SW0
1 — SW1/MRGN SW
2 — SW2
3 — SW3/SER CLK
4 — SLOT 3 INT
5 — SLOT 4 INT
6 — PDL TIMEOUT
7
C06X

# THE VERSATILE INTERFACE ADAPTER

## GENERAL

The Versatile Interface Adapter (VIA), as used in the Apple ///, is a very flexible I/O control device which minimizes the discrete control circuitry on the Main Logic Board. There are two VIAs used in the system.

Each VIA contains two 8-bit I/O ports, a serial port, and two 16-bit interval timers, as shown in the VIA Block Diagram. Each of the sections is very flexible and can be utilized in many operating modes. In the Apple ///, however,some of these modes cannot be used because of certain hardware design considerations.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves, or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register, and a pair of function control registers are provided.

Before we get into a functional description of how the VIA is used in the Apple ///, let's first go through a pin description of the it.

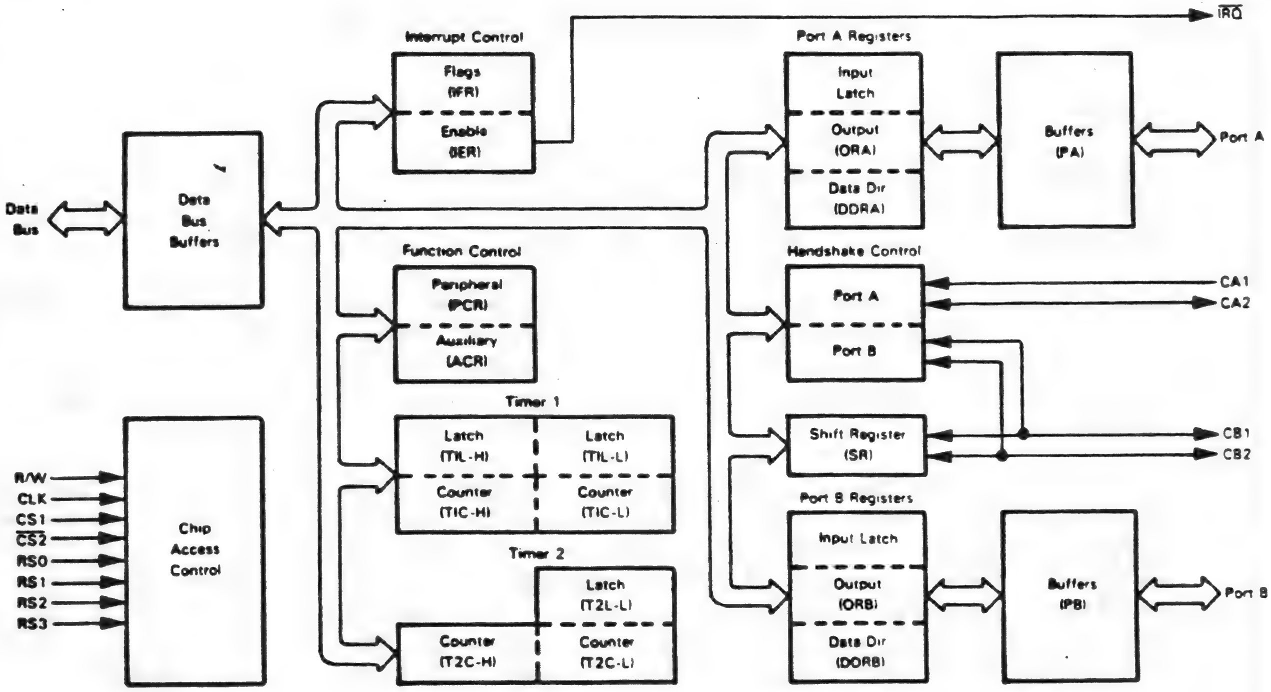
## VIA [6522] PIN DESCRIPTIONS

### RES* (Reset) (34)

The Reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters, and the shift register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc., and disables interrupting from the chip. On both VIAs this pin (34) is connected to the RESET* of the system. The system generates the reset at power on, or at depression of the Reset switch in conjunction with the Control key. (Note the latter may be disabled.)

### 02 (Input Clock) (25)

The Input Clock is the system PRE1M (PRE-1 MHZ) clock which operates at 1MHZ and is used to trigger all data transfers between the system processor and the VIA. The PRE1M, developed in the system timing circuits, is used within the device to clock the various functions of the registers and timers.


Interrupt Control
Flags (IFR)
Enable (IER)
IRQ
Port A Registers
Input Latch
Output (ORA)
Data Dir (DDRA)
Buffers (PA)
Port A
Data Bus
Data Bus Buffers
Function Control
Peripheral (PCR)
Auxiliary (ACR)
Handshake Control
Port A
Port B
CA1
CA2
Timer 1
Latch (T1L-H)
Latch (T1L-L)
Counter (T1C-H)
Counter (T1C-L)
Shift Register (SR)
CB1
CB2
R/W
CLK
CS1
CS2
RS0
RS1
RS2
RS3
Chip Access Control
Port B Registers
Input Latch
Output (ORB)
Data Dir (DDRB)
Buffers (PB)
Port B
Timer 2
Latch (T2L-L)
Counter (T2C-H)
Counter (T2C-L)

Block Diagram of the 6522 Versatile Interface Adapter

Addressing 6522 VIA Internal Registers

| **Label** | **Select Lines** | | | | **Addressed Location** |
|---|---|---|---|---|---|
| | RS3 | RS2 | RS1 | RS0 | |
| DEV | 0 | 0 | 0 | 0 | Output register for I/O Port B |
| DEV+1 | 0 | 0 | 0 | 1 | Output register for I/O Port A. with handshaking |
| DEV+2 | 0 | 0 | 1 | 0 | I/O Port B Data Direction register |
| DEV+3 | 0 | 0 | 1 | 1 | I/O Port A Data Direction register |
| DEV+4 | 0 | 1 | 0 | 0 | Read Timer 1 Counter low-order byte<br>Write to Timer 1 Latch low-order byte |
| DEV+5 | 0 | 1 | 0 | 1 | Read Timer 1 Counter high-order byte<br>Write to Timer 1 Latch high-order byte and initiate count |
| DEV+6 | 0 | 1 | 1 | 0 | Access Timer 1 Latch low-order byte |
| DEV+7 | 0 | 1 | 1 | 1 | Access Timer 1 Latch high-order byte |
| DEV+8 | 1 | 0 | 0 | 0 | Read low-order byte of Timer 2 and reset Counter interrupt<br>Write to low-order byte of Timer 2 but do not reset interrupt |
| DEV+9 | 1 | 0 | 0 | 1 | Access high-order byte of Timer 2. reset Counter interrupt on write |
| DEV+A | 1 | 0 | 1 | 0 | Serial I/O Shift register |
| DEV+B | 1 | 0 | 1 | 1 | Auxiliary Control register |
| DEV+C | 1 | 1 | 0 | 0 | Peripheral Control register |
| DEV+D | 1 | 1 | 0 | 1 | Interrupt Flag register |
| DEV+E | 1 | 1 | 1 | 0 | Interrupt Enable register |
| DEV+F | 1 | 1 | 1 | 1 | Output register for I/O Port A. without handshaking |

R/W* (Read/Write) (22)

The direction of the data transfers between the 6522 and the system processor is controlled by the R/W* line, which is driven by the Internal Read/Write, I R/W*, signal generated by the processor.

If pin 22 is low, data will be transferred out of the processor into the selected VIA register, as in a write operation.

If R/W is high, data will be transferred out of the selected 6522 register, as in a read operation.

DBO-DB7 (Data Bus) (33-26)

The eight bi-directional data bus lines (in the Internal Data Bus) are used to transfer data between the VIA and the system processor.

- During read cycles, the contents of the selected register are placed on the data bus lines and transferred into the processor.
- During the write operation, these lines are high-impedance inputs and data is transferred from the processor into the selected register.
- When the 6522 is unselected, the data bus lines are at high-impedance. These lines are connected to the Internal Data Bus and are not accessable from the outside world.

CS1, CS2* (Chip Selects) (24,23)

These two chip select lines are connected to direct decodes of the processor's address bus.

- CS1 on both VIAs is controlled by the signal CS6522, a signal which is qualified by other system consideration.
- CS2 is driven by the signal FFDX for IC at location B5, and FFEX for IC9 at location B6. The selected VIA register will be accessed when CS1 is high and CS2 is low.

RSO-RS3 (Register Selects) (38-35)

The four Register Select inputs permit the system processor to select one of the 16 internal registers, each of which performs a specific function, of the VIA as shown in the accompanying table.

IRQ (Interrupt Request) (21)

The Interrupt Request output goes low whenever an internal (to the VIA) flag is set and the corresponding interrupt enable bit is at 1. This output is "open-drain" to allow the interrupt request signal to be "wired-OR'ED" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port) (2-10)

The PA port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a data direction register.

The output is controlled by an output register. Input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers.

On standard TTL load, these lines are present in the input mode. Conversely, on standard TTL load, they will drive in the output mode.

CA1, CA2 (Peripheral A Control Lines) (40,39)

The two PA control lines can act as interrupt inputs (as used in the Apple ///) or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit.

PB0-PB7 (Peripheral B Port) (11-17)

The PB port consists of 8 bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port.

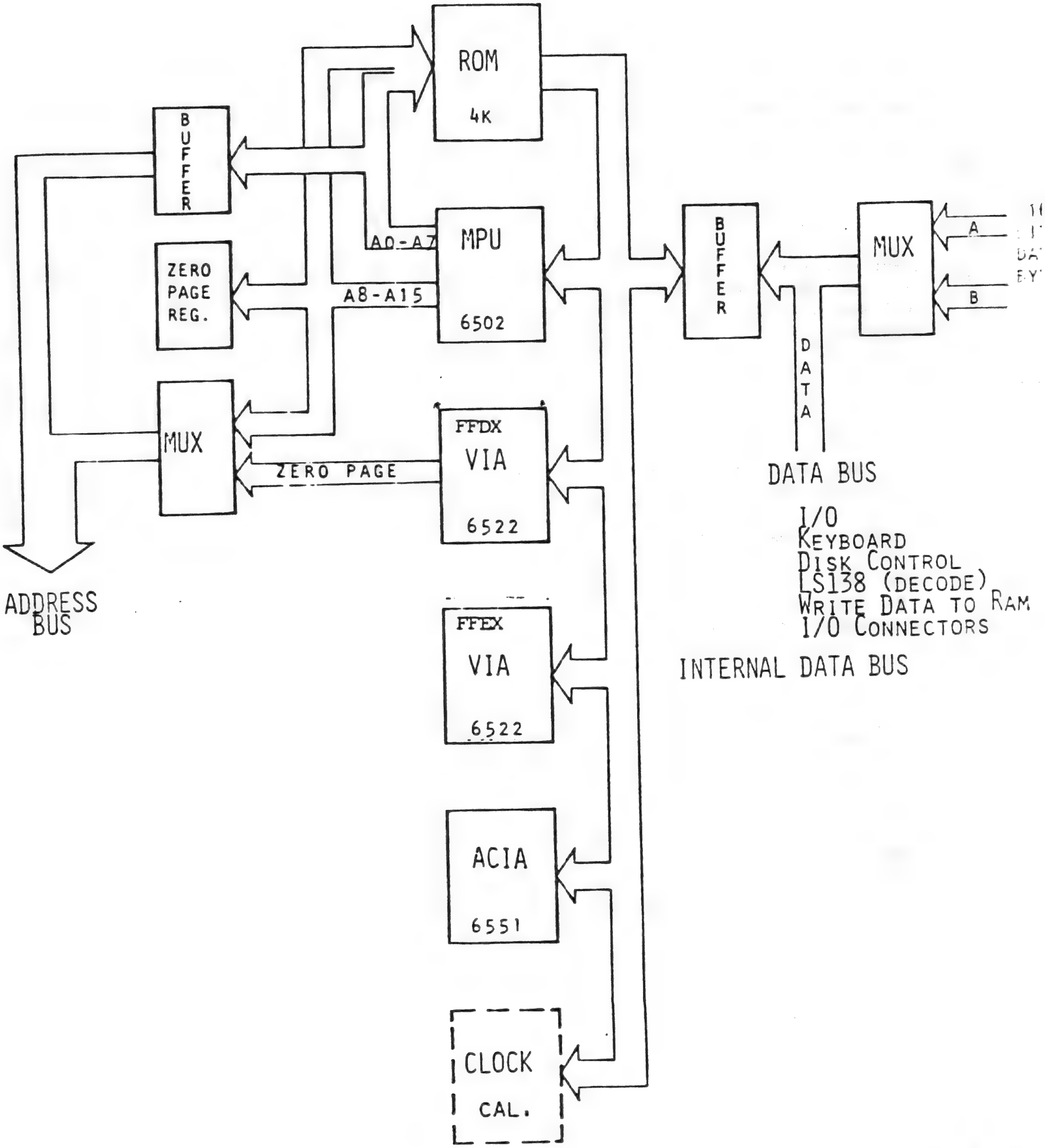
The polarity of the PB7 output signal can be controlled by one of the interval timers, while the second timer can be programmed to count pulses on the PB6 pin.

Peripheral B lines represent one TTL load in the input mode and drive one standard load in the output mode.

CB1, CB2 (Peripheral B Control Lines) (18-19)

The PB control lines act as interrupt inputs or as handshake outputs. As with the CA lines, each line controls an interrupt flag.

These lines also act as a serial port under control of the Shift Register. They have loading and driving characteristics identical to the CA control lines.


ROM
4K
BUFFER
MPU
6502
A0-A7
A8-A15
ZERO PAGE REG.
MUX
FFDX
VIA
6522
ZERO PAGE
FFEX
VIA
6522
ACIA
6551
CLOCK
CAL.
ADDRESS BUS
BUFFER
MUX
A
B
DATA
DATA BUS
I/O
KEYBOARD
DISK CONTROL
LS138 (DECODE)
WRITE DATA TO RAM
I/O CONNECTORS
INTERNAL DATA BUS

## VIA FUNCTIONAL DESCRIPTION

### Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register for specifying whether the Peripheral pins are to act as inputs or outputs.

- A "0" in a bit of the DDR causes the corresponding peripheral pin to act as an input.
- A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register and a bit in the Input Register. When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the output Register. A one in the ORX causes the output to go high; a zero causes the output to go low.

Data may be written into ORX bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

The IRB Register operation is similar to that of the IRA. For pins programmed as outputs, however, there is a difference. When reading the IRB, it is the bit stored in the ORB that is sensed. That means the buffering and gating on the two ports differ in respect to pins programmed as outputs.

See the figures below detailing the data bytes programmed into the DDRs and the two control registers for each of the VIAs. Compare these with the environments of each device.

### Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16 bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at the rate of PRE1M.

Upon reaching zero, an interrupt flag will be set; if the interrupt is enabled, the IRQ* will go low. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement.

In addition, the timer may be programmed to invert the output signal on a peripheral pin each tme it "times out." Each of these modes is discussed below.

### Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the write T1C-H (FFD5, FFE5) operation and generation of the processor interrupt is a direct function of the data loaded into the timer.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it is necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation.

When the processor writes into the high order counter

- the T1 interrupt flag is cleared;
- the contents of the low order latch are transferred into the low order counter;
- the timer again begins to decrement at the PRE1M rate.

After the timer reaches its time out, it continues to decrement until it is reset with the proper write operation.

The processor may read the current count of the timer to determine how long it has been since the interrupt has been set. Reading the counter does not reset the interrupt flag or the timer.

### Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts. These interrupts are accomplished in the "free-running mode."

In the free-running mode, the interrupt flag is set each time the counter reaches zero. However, instead of continuing to decrement from zero, the timer automatically reloads the contents of the high and low latches, and continues to decrement from there. In this mode, the interrupt flag can be cleared by writing T1C-H, or reading T1C-L, or by writing directly to the interrupt flag.

It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. All of the interval timers are "retriggerable." Re-writing the counter will always re-initialize the time-out period.

### Timer 2 Operation

Timer 2 operates as an interval timer in the one-shot mode only, or as a counter of negative pulses on the PB6 peripheral pin. A single bit in the ACR is provided for this mode selection.

Timer 2 is comprised of a write-only low order latch, a read-only low order counter, and a read/write high order counter.

### Timer 2 One Shot-Mode

As an interval timer, T2 operates very much like T1 in the one-shot mode. Setting of the interrupt flag, however, will be disabled after the first time out, and it will not be set again until the write T2C-H operation.

The flag can be reset by reading T2C-L, or by writing T2C-H.

### Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on the P6 pin. This is accomplished by first loading a number into T2, which clears the interrupt flag and allows the counter to be decremented by the pulses on PB6. The interrupt flag will be set when T2 is decremented to zero. The counter will continue to decrement.

Note that it is necessary to rewrite the timer to re-enable the subsequent interrupt flags.

### Shift Register Operation

The Shift Register performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which set the various register modes are located in the ACR. In total, there are eight modes for this register. The primary use of the shift register is control of the serial printer port.

In the FFEX VIA, the shift register can be activated to "count" 8 VBL (Vertical Blanking) pulses. The shift register sets its interrupt flag each time it completes 8 shifts.

Refer to the figure below for descriptions of the various modes of the shift register.

### Interrupt Operation

Controlling interrupts within the VIA involves three principal operations. These are:

- o flagging the interrupts
- o enabling the interrupts
- o signalling the processor that an interrupt condition has occurred.

Interrupt flags are set by interrupting conditions which exist within the chip, or on inputs to the chip. These flags normally remain set until the interrupt has been serviced by the processor. To determine the source of an interrupt, the processor must examine these flags in order from highest to lowest priority.

Procedure:

1. Read the flag register into the accumulator.
2. Shift it right or left.
3. Use conditional branch instructions to detect an active interrupt.

Associated with each flag bit is an enable bit. This can be set or cleared by the processor to enable or disable the flag respectively. If a flag bit is enabled and set, it will cause the IRQ* output to go low, thus sending a direct request to the processor. In addition, bit 7 of the flag register is set to allow quick determination of which chip contains an interrupt condition.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register controls are applied to the chip, the contents of the IFR are placed on the Data Bus. Bit 7 indicates the condition of the IRQ output, however it cannot be directly cleared; all other bits must be cleared in order for this bit to become inactive.

For each interrupt flag in the IFR there is a corresponding bit in the Interrupt Enable Register. This is accomplished by writing to the IER. There are two steps to consider: the enabling write cycle and the disabling write cycle. The cycle is determined by the logic state of bit 7:

- o If bit 7 and the corresponding 0-6 bits are at "1", the 0-6 bits enable their matching flag.
- o If bit 7 is a 0, then the 0-6 bits containing a "1" disable the matching flag.

Refer to the figures to see the data byte configuration and device.

## 6522 VIA Environment and Control

The description so far has been very general and has not completely detailed the functions of the two VIAs within the Apple ///. However, one must be familiar with the many registers and modes to understand how the VIA is utilized and how it can be configured for various operations.

The following figures and tables detail the environment and address locations of each of the registers and I/O pins for the two chips. (Many of the signals are common controls or busses; their descriptions relate to both devices.)

### IDO-ID7

The data bus pins of the VIA are connected to the associated pins of the Internal Data bus. When the chip is properly addressed and selected, each of the various registers may be accessed for reading or writing data, control bytes, status or timer states. It is this bus through which all data passes to the system and/or processor.

### Reset

The RES pin is connected to the RESET line. The system generates the reset at Power On or when the Reset switch is depressed with the Control key.

(Note: the Control key may be software disabled.)

### I R/W*

The R/W* pin is connected directly to the processor´s internal Read/Write line. This signal cannot be accessed from the outside world. It is obviously used to control the direction of the data to or from the device.

### PRE1M

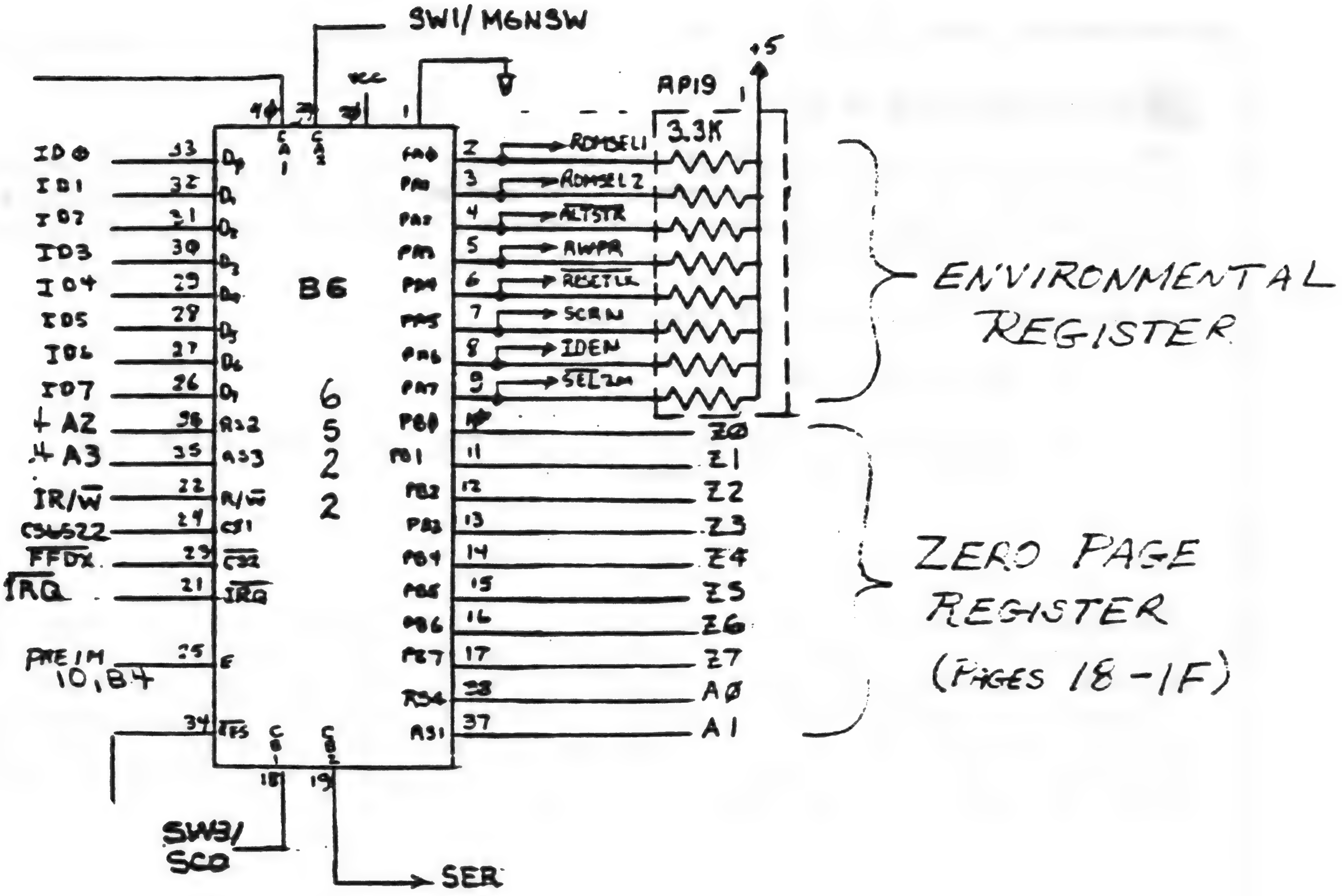
The 02 clock pin is driven by the PRE1M signal developed in the system timing circuits. It is used within the device to clock the various functions of the registers and timers.

### CS6522

This signal is developed under Rom decode of various address states or ranges and other mode selections, and drives the CS1 line of both VIAs.

### A0-A3

The processor´s address lines directly drive the Register Select input lines.


SW1/ M6NSW
+5
RP19
3.3K
1
B6
6522
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
A2
A3
IR/W̄
CS6522
FFDX
IRQ
PREIM 10,B4
D0
D1
D2
D3
D4
D5
D6
D7
RS2
RS3
R/W̄
CS1
CS2
IRQ
E
RES
CA1
CA2
CB1
CB2
Vcc
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
RS0
RS1
ROMSEL1
ROMSEL2
ALTSTR
RWPR
RESETLK
SCRN
IDEN
SEL2M
Z0
Z1
Z2
Z3
Z4
Z5
Z6
Z7
A0
A1
ENVIRONMENTAL REGISTER
ZERO PAGE REGISTER (PAGES 18 - 1F)
SW3/ SCO
SER

| ADDRESS | Register Number | RS Coding | | | | Register Desig. | Description | |
|---|---|---|---|---|---|---|---|---|
| | | RS3 | RS2 | RS1 | RS0 | | Write | Read |
| FFD0 | 0 | 0 | 0 | 0 | 0 | ORB/IRB | Output Register "B" | Input Register "B" |
| FFD1 | 1 | 0 | 0 | 0 | 1 | ORA/IRA | Output Register "A" | Input Register "A" |
| FFD2 | 2 | 0 | 0 | 1 | 0 | DDRB | Data Direction Register "B" | |
| FFD3 | 3 | 0 | 0 | 1 | 1 | DDRA | Data Direction Register "A" | |
| FFD4 | 4 | 0 | 1 | 0 | 0 | T1C-L | T1 Low-Order Latches | T1 Low-Order Counter |
| FFD5 | 5 | 0 | 1 | 0 | 1 | T1C-H | T1 High-Order Counter | |
| FFD6 | 6 | 0 | 1 | 1 | 0 | T1L-L | T1 Low-Order Latches | |
| FFD7 | 7 | 0 | 1 | 1 | 1 | T1L-H | T1 High-Order Latches | |
| FFD8 | 8 | 1 | 0 | 0 | 0 | T2C-L | T2 Low-Order Latches | T2 Low-Order Counter |
| FFD9 | 9 | 1 | 0 | 0 | 1 | T2C-H | T2 High-Order Counter | |
| FFDA | A 10 | 1 | 0 | 1 | 0 | SR | Shift Register | |
| FFDB | 11 | 1 | 0 | 1 | 1 | ACR | Auxiliary Control Register | |
| FFDC | C 12 | 1 | 1 | 0 | 0 | PCR | Peripheral Control Register | |
| FFDD | 13 | 1 | 1 | 0 | 1 | IFR | Interrupt Flag Register | |
| FFDE | 14 | 1 | 1 | 1 | 0 | IER | Interrupt Enable Register | |
| FFDF | 15 | 1 | 1 | 1 | 1 | ORA/IRA | Same as Reg 1 Except No "Handshake" | |

SY6522 Internal Register Summary

These four addresses, along with the two chip select lines, activate the chip for access to and from the data bus. You can see that the decimal equivalent of the address (Register Select) lines equals the register number, as detailed in the port address tables.

To determine the complete I/O location:

- Express the A0-A7 bits in Hex
- Substitute the Hex expression for the "x" in the signal name applied to the CS2 input.

IRQ*

The Interrupt Request line is a wire OR´ED bus, shared with the other LSI devices within the system which directly interrupt the processor. The VIA can generate an interrupt due to internal status and can be configured to interrupt on various input conditions. Each VIA provides indirect interrupts to the processor for the other devices in the system, including the slot interrupts. By polling the VIAs, the processor can quickly determine which device or group of devices needs servicing.

## VIA (FFDX)

This VIA has the following responsibilities:

- Environmental Register
- Zero Page Register
- Global Interrupt Request
- Serial Data Port Interrupt & Clocking (Silentype)

The signals of the IC at location B6 which are not common to both 6522s are either the port I/Os or the chip select line, CS2.

FFDX

This signal comes from the Device Select logic, and is true for the 16 address states, FFD0 through FFDF.

The table below shows how the signal FFDX (CS2) and the Address Lines on the Register Select Inputs access each of the 16 registers within the VIA.

## Port A Description

The ORA for this device is also called the "Environmental Register" by the system. It is programmed to all outputs, and contains various control mode states which may be software modified.

PA0 and PA1 are used as software switches to control which set of Roms are to be used by the system, and also to indicate there is an expanded set of Rom in the system.

PA2 provides the software switch that enables the Apple /// to switch between two memory stacks.

PA3 is a software switch which will enable or disable the system for writing into the Ram. It can be set for entire banks or it can be set at will to disallow writing into memory.

PA4 is a software switch which will cause the function of the Reset switch to be ignored, and will simultaneously disable the Non-Maskable Interrupts from the I/O slots.

PA5 contains the switch "Scrn" (Screen) which is used to modify the Blanking signal.

## Global IRQ

The CA1 line is connected to "OR" function of the slot IRQs. If any slot is requesting an interrupt, this line will toggle. The VIA then generates an IRQ and sets the associated Interrupt flag.

## Swl/Mgnsw

This line connected to the CA2 line can be programmed to cause an interrupt on either edge of transition. It could be used to have a Function Only run while the switch is depressed, or vice versa.

## SCO/SER

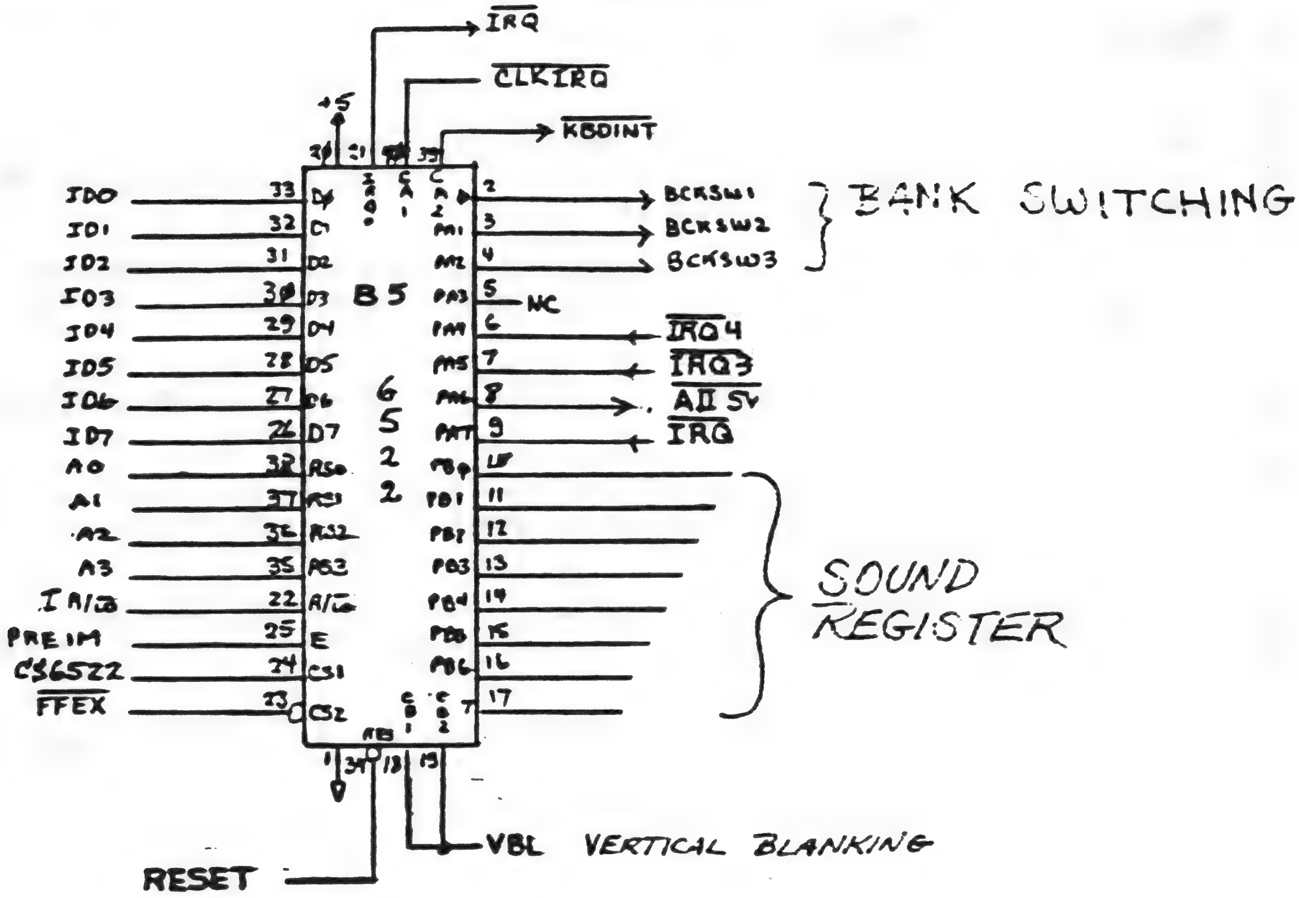
These two signals form a very elementary serial data port. They are usually programmed as data, and strobe to a serial RO printer.

The port may also be configured as a serial input register or simply as interrupts for the two external lines.

SCO/SER are connected to CB1 and CB2 respectively.

## Z0-Z7 (Zero Page Register)

# VIA FFEX


IRQ
CLKIRQ
+5
KBDINT
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
A0
A1
A2
A3
IR/W
PREIM
CS6522
FFEX
B5
6522
BCKSW1
BCKSW2
BCKSW3
BANK SWITCHING
NC
IRQ4
IRQ3
AII SV
IRQ
SOUND REGISTER
RESET
VBL VERTICAL BLANKING

| ADDRESS | Register Number | RS Coding RS3 | RS2 | RS1 | RS0 | Register Desig. | Description Write | Read |
|---|---|---|---|---|---|---|---|---|
| FFE0 | 0 | 0 | 0 | 0 | 0 | ORB/IRB | Output Register "B" | Input Register "B" |
| FFE1 | 1 | 0 | 0 | 0 | 1 | ORA/IRA | Output Register "A" | Input Register "A" |
| FFE2 | 2 | 0 | 0 | 1 | 0 | DDRB | Data Direction Register "B" | |
| FFE3 | 3 | 0 | 0 | 1 | 1 | DDRA | Data Direction Register "A" | |
| FFE4 | 4 | 0 | 1 | 0 | 0 | T1C-L | T1 Low-Order Latches | T1 Low-Order Counter |
| FFE5 | 5 | 0 | 1 | 0 | 1 | T1C-H | T1 High-Order Counter | |
| FFE6 | 6 | 0 | 1 | 1 | 0 | T1L-L | T1 Low-Order Latches | |
| FFE7 | 7 | 0 | 1 | 1 | 1 | T1L-H | T1 High-Order Latches | |
| FFE8 | 8 | 1 | 0 | 0 | 0 | T2C-L | T2 Low-Order Latches | T2 Low-Order Counter |
| FFE9 | 9 | 1 | 0 | 0 | 1 | T2C-H | T2 High-Order Counter | |
| FFEA | 10 | 1 | 0 | 1 | 0 | SR | Shift Register | |
| FFEB | 11 | 1 | 0 | 1 | 1 | ACR | Auxiliary Control Register | |
| FFEC | 12 | 1 | 1 | 0 | 0 | PCR | Peripheral Control Register | |
| FFED | 13 | 1 | 1 | 0 | 1 | IFR | Interrupt Flag Register | |
| FFEE | 14 | 1 | 1 | 1 | 0 | IER | Interrupt Enable Register | |
| FFEF | 15 | 1 | 1 | 1 | 1 | ORA/IRA | Same as Reg 1 Except No "Handshake" | |

The PB port is referred to as the Zero Page Register. In other words, its primary function is to store the current "Zero Page" of the memory. The Apple /// is capable of moving the Zero Page, a feature which greatly enhances the flexibility of the system.

The PB port has a secondary function; it also serves as the address register for the Real Time Clock. The RTC must have the addresses stable for an extended period of time, so instead of adding another latch in the hardware, the designers use this port for control.

Note that each time the port is used for the RTC function it must be restored to the current Zero Page setting.

## VIA (FFEX)

This VIA aids in providing the following:

- Bank Switching
- Sound Register
- Interrupt Recognition-clock, keyboard

The signals connected to the VIA located at B5 which are not common to both VIAs are:

- the A and B port I/Os,
- the port control lines, and
- the CS2 line.

### FFEX

This signal corresponds to FFDX in that it is true for a group of 16 addresses. See the corresponding table for the complete detail of the register access locations.

### Port A Description

The PA0-PA2 lines are configured as outputs and contain the software switches for the Ram banks. Currently, the system segregates the 128K memory into three banks. The decimal decode of the binary bit weight reveals the bank.

The PA4-PA7 lines are configured as inputs. Slot 1 and 2 IRQs, the Solid Apple switch, and the IRQ line itself form the respective inputs.

If it´s interrupted, the processor will poll the VIAs first to get a quick look at most of the system. It can then identify and service the requesting device faster, since it doesn´t need to poll each individual device.

The processor can, at certain times, read this port for the status of the special Apple switch on the keyboard without disturbing the keyboard circuit.

The IRQ* signal is wrapped around to the PA7 line for special diagnostic purposes.

### CLK IRQ*

The Real Time Clock's interrupt is connected to the CA1 line, which is programmed to be a negative edge active input. When the clock generates an interrupt, it will set the IRA flag in the IFR. The PA port is conditioned for non-latching, however, resulting in a basically independent interrupt for the clock.

### Keyboard Interrupt

The keyboard's interrupt is connected to the CA2 input, which is programmed to be an independent negative edge interrupt. It will set Bit 0 in the IFR and cause the IRQ* line to go low.

Note: The keyboard can, for the most part, be disabled by disabling the interrupt flag for the CA2 line.

### VBL (Vertical Blanking)

This input can perform two functions, depending on how the CB1, CB2, and Shift Register are programmed.

- The system may want to be interrupted at each vertical blanking cycle. If so, you would program the CB2 line to be an independent interrupt OR let it strobe the IPB and set the corresponding bit flag.
- The system may want to synchronize an operation to the display, but may not want to be interrupted at each VBL. If this is the case, the system can configure the Shift Register to count 8 occurrences of the VBL signal. An interrupt will then occur after each set of 8 Vertical Blanking cycles (about once every second), in sync with the display scan.

### PB Port Description

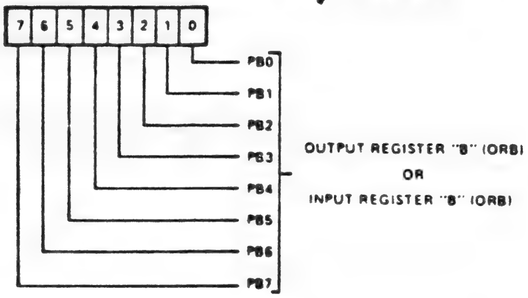
The first 6 lines of the B port are configured to be outputs. They are inputs to the sound Generator.

- The tone generated at the speaker can be varied by changing the bit values of these lines.
- There are 127 possible tone combinations; the missing one turns the tone off completely.

PB6 is connected to the I/O Count line. Depending on the device in the slots, the VIA may be programmed to count a certain number of pulses generated or to determine that only one pulse occurred. Either way, the VIA will generate an IRQ and set the appropriate bit flag.

The last bit is used to monitor the NMI (Non Maskable Interrupt) line generated by the devices in the I/O slots.

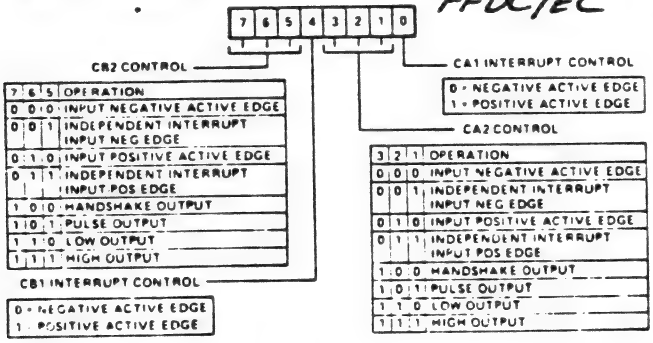
REG 0 – ORB/IRB **FFD0/E0**


7
6
5
4
3
2
1
0
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
OUTPUT REGISTER "B" (ORB)
OR
INPUT REGISTER "B" (ORB)

| Pin Data Direction Selection | WRITE | READ |
|---|---|---|
| DDRB = "1" (OUTPUT) | MPU writes Output Level (ORB) | MPU reads output register bit in ORB. Pin level has no affect |
| DDRB = "0" (INPUT) (Input latching disabled) | MPU writes into ORB, but no effect on pin level, until DDRB changed | MPU reads input level on PB pin |
| DDRB = "0" (INPUT) (Input latching enabled) | | MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition |

Figure 9. Output Register B (ORB), Input Register B (IRB)

REG 12 – PERIPHERAL CONTROL REGISTER FFDC/EC


7
6
5
4
3
2
1
0
CB2 CONTROL
CA1 INTERRUPT CONTROL
CA2 CONTROL
CB1 INTERRUPT CONTROL

| 7 | 6 | 5 | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | INPUT NEGATIVE ACTIVE EDGE |
| 0 | 0 | 1 | INDEPENDENT INTERRUPT INPUT NEG EDGE |
| 0 | 1 | 0 | INPUT POSITIVE ACTIVE EDGE |
| 0 | 1 | 1 | INDEPENDENT INTERRUPT INPUT POS EDGE |
| 1 | 0 | 0 | HANDSHAKE OUTPUT |
| 1 | 0 | 1 | PULSE OUTPUT |
| 1 | 1 | 0 | LOW OUTPUT |
| 1 | 1 | 1 | HIGH OUTPUT |

CB1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA1 INTERRUPT CONTROL

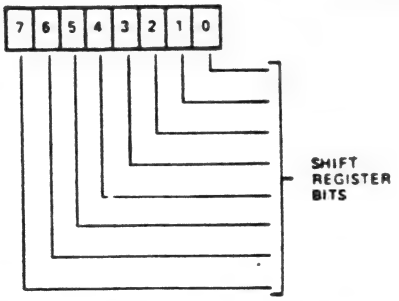
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA2 CONTROL

| 3 | 2 | 1 | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | INPUT NEGATIVE ACTIVE EDGE |
| 0 | 0 | 1 | INDEPENDENT INTERRUPT INPUT NEG EDGE |
| 0 | 1 | 0 | INPUT POSITIVE ACTIVE EDGE |
| 0 | 1 | 1 | INDEPENDENT INTERRUPT INPUT POS EDGE |
| 1 | 0 | 0 | HANDSHAKE OUTPUT |
| 1 | 0 | 1 | PULSE OUTPUT |
| 1 | 1 | 0 | LOW OUTPUT |
| 1 | 1 | 1 | HIGH OUTPUT |

Figure 14. CA1, CA2, CB1, CB2 Control

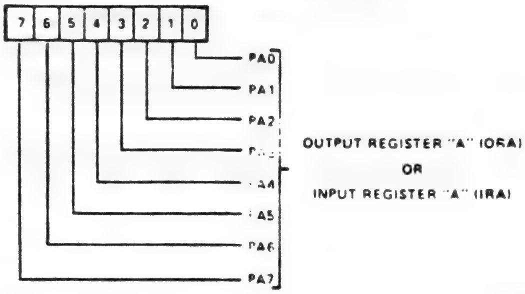
REG 10 – SHIFT REGISTER FFEA/DA


7
6
5
4
3
2
1
0
SHIFT
REGISTER
BITS

NOTES:

1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

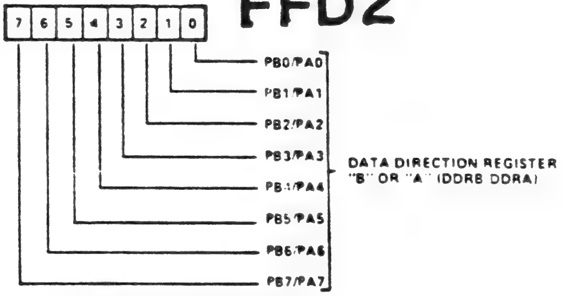
REG 1 – ORA/IRA **FFE1/D1**


7
6
5
4
3
2
1
0
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
OUTPUT REGISTER "A" (ORA)
OR
INPUT REGISTER "A" (IRA)

| Pin Data Direction Selection | WRITE | READ |
|---|---|---|
| DDRA = "1" (OUTPUT) (Input latching disabled) | MPU writes Output Level (ORA) | MPU reads level on PA pin |
| DDRA = "1" (OUTPUT) (Input latching enabled) | | MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition |
| DDRA = "0" (INPUT) (Input latching disabled) | MPU writes into ORA, but no effect on pin level, until DDRA changed | MPU reads level on PA pin |
| DDRA = "0" (INPUT) (Input latching enabled) | | MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition |

Figure 10. Output Register A (ORA), Input Register A (IRA)

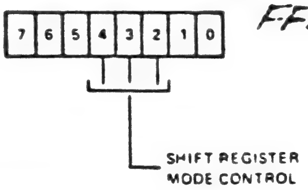
REG 2 (DDRB) AND REG 3 (DDRA) **FFD2**


7
6
5
4
3
2
1
0
PB0/PA0
PB1/PA1
PB2/PA2
PB3/PA3
PB4/PA4
PB5/PA5
PB6/PA6
PB7/PA7
DATA DIRECTION REGISTER "B" OR "A" (DDRB DDRA)

"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT.

REG 11 – AUXILIARY CONTROL REGISTER FFDB/EB


7
6
5
4
3
2
1
0
SHIFT REGISTER MODE CONTROL

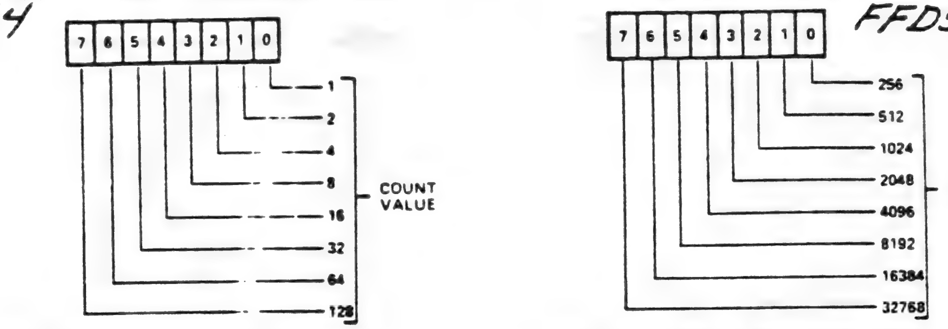
| 4 | 3 | 2 | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | DISABLED |
| 0 | 0 | 1 | SHIFT IN UNDER CONTROL OF T2 |
| 0 | 1 | 0 | SHIFT IN UNDER CONTROL OF $\Phi_2$ |
| 0 | 1 | 1 | SHIFT IN UNDER CONTROL OF EXT CLK |
| 1 | 0 | 0 | SHIFT OUT FREE RUNNING AT T2 RATE |
| 1 | 0 | 1 | SHIFT OUT UNDER CONTROL OF T2 |
| 1 | 1 | 0 | SHIFT OUT UNDER CONTROL OF $\Phi_2$ |
| 1 | 1 | 1 | SHIFT OUT UNDER CONTROL OF EXT CLK |

Figure 22. SR and ACR Control Bits

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

FFD4/E4

FFD5/E5


REG 4 – TIMER 1 LOW-ORDER COUNTER
7 6 5 4 3 2 1 0
1
2
4
8
16
32
64
128
COUNT VALUE
REG 5 – TIMER 1 HIGH-ORDER COUNTER
7 6 5 4 3 2 1 0
256
512
1024
2048
4096
8192
16384
32768
COUNT VALUE

WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

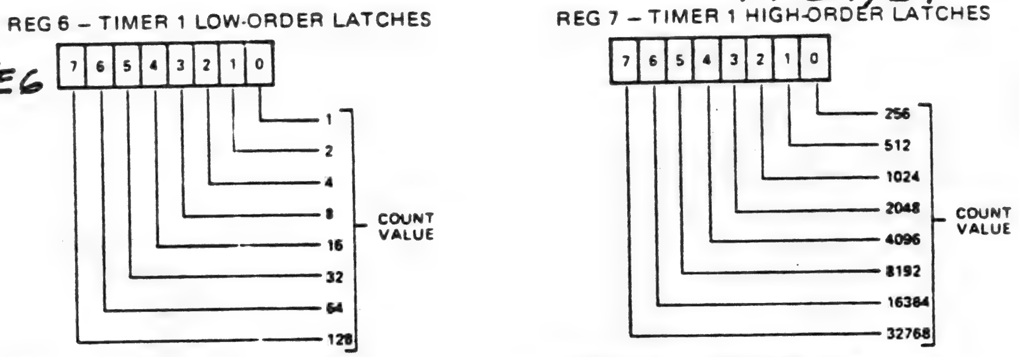
WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

FFD7/E7

FFD6/E6


REG 6 – TIMER 1 LOW-ORDER LATCHES
7 6 5 4 3 2 1 0
1
2
4
8
16
32
64
128
COUNT VALUE
REG 7 – TIMER 1 HIGH-ORDER LATCHES
7 6 5 4 3 2 1 0
256
512
1024
2048
4096
8192
16384
32768
COUNT VALUE

WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

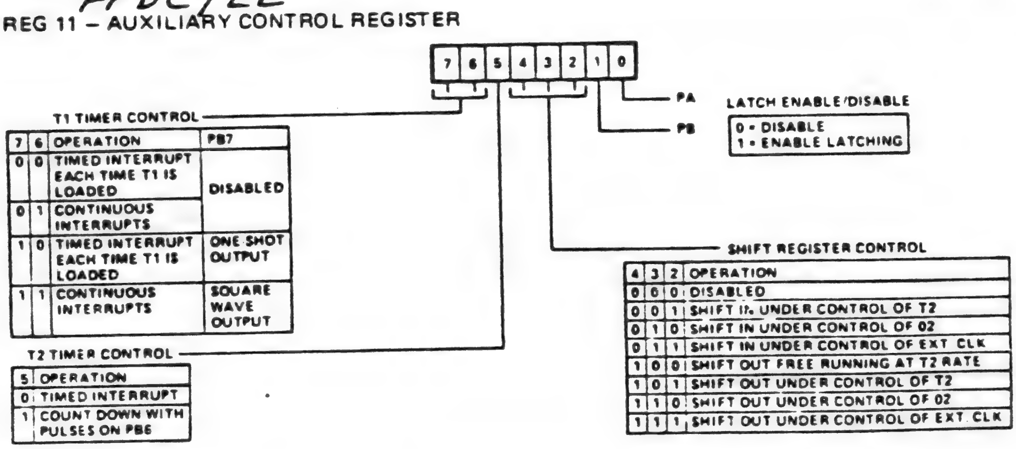
READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

FFDC/EC


REG 11 – AUXILIARY CONTROL REGISTER
7 6 5 4 3 2 1 0
PA
PB
LATCH ENABLE/DISABLE
T1 TIMER CONTROL
T2 TIMER CONTROL
SHIFT REGISTER CONTROL

LATCH ENABLE/DISABLE

0 = DISABLE
1 = ENABLE LATCHING

T1 TIMER CONTROL

| 7 | 6 | OPERATION | PB7 |
|---|---|---|---|
| 0 | 0 | TIMED INTERRUPT EACH TIME T1 IS LOADED | DISABLED |
| 0 | 1 | CONTINUOUS INTERRUPTS | |
| 1 | 0 | TIMED INTERRUPT EACH TIME T1 IS LOADED | ONE SHOT OUTPUT |
| 1 | 1 | CONTINUOUS INTERRUPTS | SQUARE WAVE OUTPUT |

T2 TIMER CONTROL

| 5 | OPERATION |
|---|---|
| 0 | TIMED INTERRUPT |
| 1 | COUNT DOWN WITH PULSES ON PB6 |

SHIFT REGISTER CONTROL

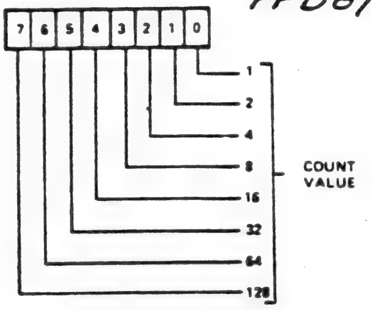
| 4 | 3 | 2 | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | DISABLED |
| 0 | 0 | 1 | SHIFT IN UNDER CONTROL OF T2 |
| 0 | 1 | 0 | SHIFT IN UNDER CONTROL OF 02 |
| 0 | 1 | 1 | SHIFT IN UNDER CONTROL OF EXT. CLK |
| 1 | 0 | 0 | SHIFT OUT FREE RUNNING AT T2 RATE |
| 1 | 0 | 1 | SHIFT OUT UNDER CONTROL OF T2 |
| 1 | 1 | 0 | SHIFT OUT UNDER CONTROL OF 02 |
| 1 | 1 | 1 | SHIFT OUT UNDER CONTROL OF EXT. CLK |

Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

### REG 8 – TIMER 2 LOW-ORDER COUNTER

FFD8/E8

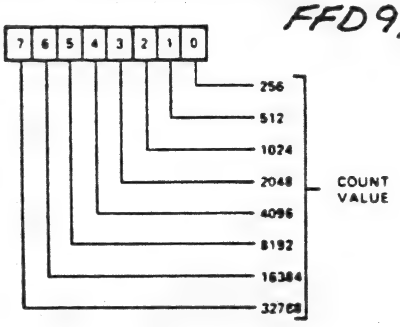

7
6
5
4
3
2
1
0
1
2
4
8
16
32
64
128
COUNT VALUE

WRITE – 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

### REG 9 – TIMER 2 HIGH-ORDER COUNTER

FFD9/E9

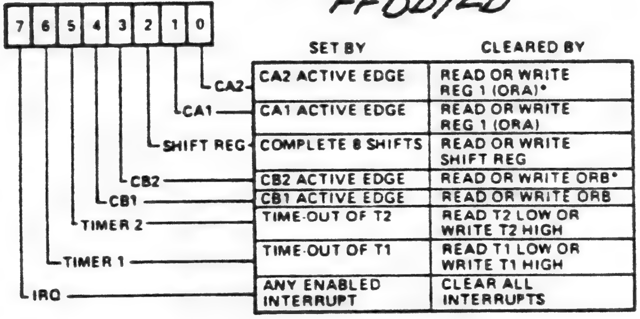

7
6
5
4
3
2
1
0
256
512
1024
2048
4096
8192
16384
32768
COUNT VALUE

WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ – 8 BITS FROM T2 HIGH ORDER COUNTER TRANSFERRED TO MPU.

### REG 13 – INTERRUPT FLAG REGISTER

FFDD/ED

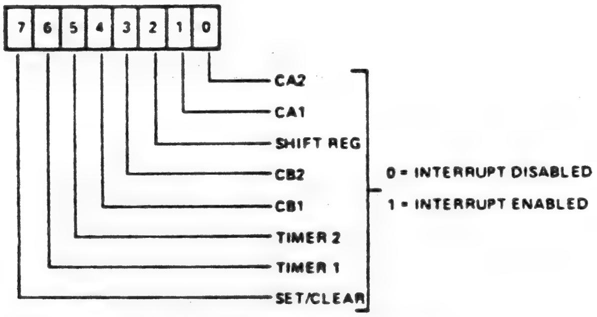


| | SET BY | CLEARED BY |
|---|---|---|
| CA2 | CA2 ACTIVE EDGE | READ OR WRITE REG 1 (ORA)* |
| CA1 | CA1 ACTIVE EDGE | READ OR WRITE REG 1 (ORA) |
| SHIFT REG | COMPLETE 8 SHIFTS | READ OR WRITE SHIFT REG |
| CB2 | CB2 ACTIVE EDGE | READ OR WRITE ORB* |
| CB1 | CB1 ACTIVE EDGE | READ OR WRITE ORB |
| TIMER 2 | TIME-OUT OF T2 | READ T2 LOW OR WRITE T2 HIGH |
| TIMER 1 | TIME-OUT OF T1 | READ T1 LOW OR WRITE T1 HIGH |
| IRQ | ANY ENABLED INTERRUPT | CLEAR ALL INTERRUPTS |

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

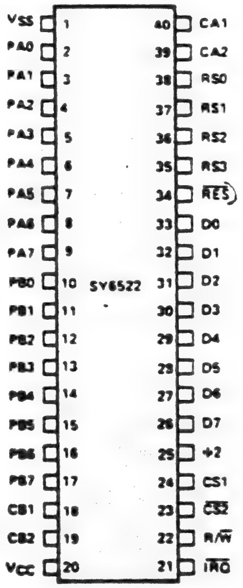
Figure 25. Interrupt Flag Register (IFR)

### REG 14 – INTERRUPT ENABLE REGISTER


7
6
5
4
3
2
1
0
CA2
CA1
SHIFT REG
CB2
CB1
TIMER 2
TIMER 1
SET/CLEAR
0 = INTERRUPT DISABLED
1 = INTERRUPT ENABLED

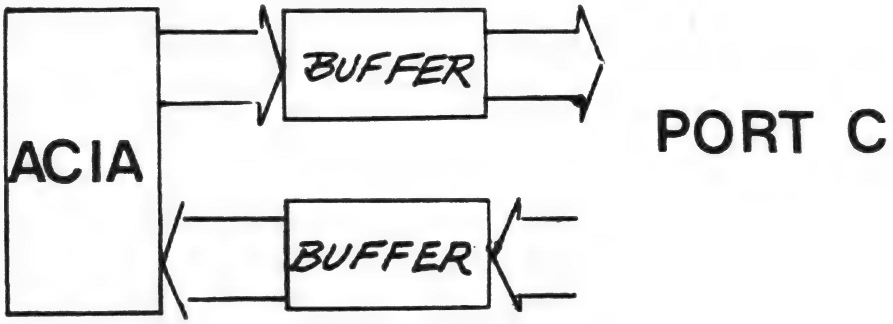
NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "0" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

### PIN CONFIGURATION


VSS 1
PA0 2
PA1 3
PA2 4
PA3 5
PA4 6
PA5 7
PA6 8
PA7 9
PB0 10
PB1 11
PB2 12
PB3 13
PB4 14
PB5 15
PB6 16
PB7 17
CB1 18
CB2 19
Vcc 20
SY6522
40 CA1
39 CA2
38 RS0
37 RS1
36 RS2
35 RS3
34 RES
33 D0
32 D1
31 D2
30 D3
29 D4
28 D5
27 D6
26 D7
25 φ2
24 CS1
23 CS2
22 R/W
21 IRQ

## THE 6551 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER

As you know, the Apple /// can be used to communicate to all devices that use the RS-232-C standard communications format. This means the Apple /// can communicate with letter-quality printers, modems, high speed data collection devices, and other computers. The Apple /// has a built in Asynchronous Communications Interface Adapter (ACIA). It is located at addresses COFO through COF3. This device is solely for use as a serial port input/output controller. This RS-232-C protocol, specified by the Electrical Industries Association (EIA), is provided at port C connector through two buffer devices as shown below.



The 6551 contains seven registers and five control circuits dealing with the control, timing, and interrupt logic of transmitting amd receiving data through the serial EIA port. A block diagram of the 6551 ACIA is shown in Figure 1.

Before using the 6551, the system (or programmer) must initialize it for the I/O mode. Once initialized it will be set to transmit and/or receive data within the parameters set in the control bytes.

The Apple /// I/O addresses for data and control are presented in the following discussions. The function of the data byte (depending on location) will also be shown. The characters in parentheses next to each register represent the function of the associated pin of the ACIA (i.e. R=Read,W=Write).

RECEIVE DATA REGISTER (RxD)

The Receive Data Register is accessed with I/O location COFO (r). The contents of the Receive Data Register will be the data bits of the completely received serial input character. This register is used as temporary data storage for the 6551 receive circuit. The first data bit received will be the LSB of the data byte (Bit 0).

COFO (R) RECEIVE DATA REGISTER

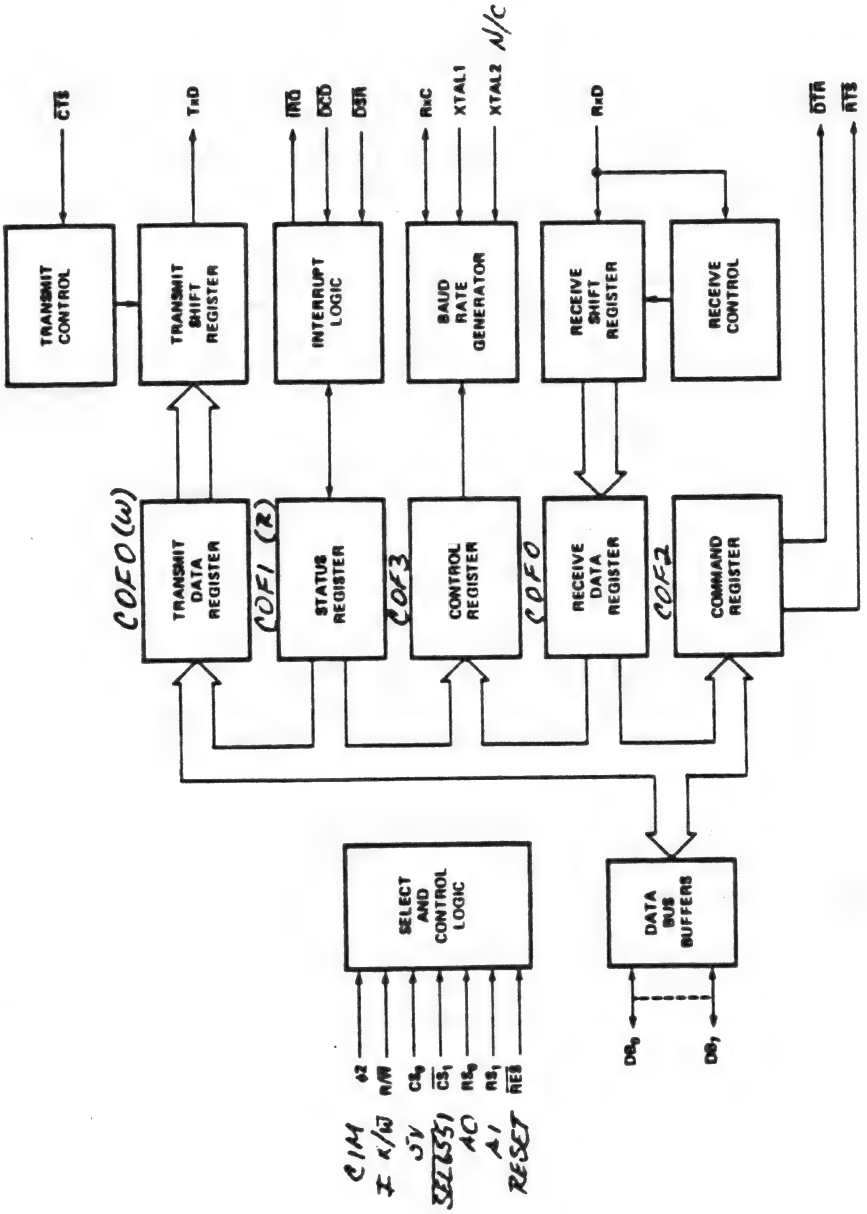

$\overline{CTS}$
TxD
$\overline{IRQ}$
$\overline{DCD}$
$\overline{DSR}$
RxC
XTAL1
XTAL2
N/C
RxD
$\overline{DTR}$
$\overline{RTS}$
TRANSMIT CONTROL
TRANSMIT SHIFT REGISTER
INTERRUPT LOGIC
BAUD RATE GENERATOR
RECEIVE SHIFT REGISTER
RECEIVE CONTROL
COF0 (W)
TRANSMIT DATA REGISTER
COF1 (R)
STATUS REGISTER
COF3
CONTROL REGISTER
COF0
RECEIVE DATA REGISTER
COF2
COMMAND REGISTER
SELECT AND CONTROL LOGIC
DATA BUS BUFFERS
$\phi 2$
R/W
$CS_0$
$\overline{CS_1}$
$RS_0$
$RS_1$
$\overline{RES}$
C1M
I R/W
5V
$\overline{SEL6551}$
A0
A1
RESET
$DB_0$
$DB_7$

FIG 1

THE ACIA BLOCK DIAGRAM

## TRANSMIT DATA REGISTER (TxD)

To load a byte to be transmitted out the serial EIA port, I/O location C0F0 (w) must be accessed. The LSB will be the first data bit transmitted.

C0F0 (w) TRANSMIT DATA REGISTER (w)

## STATUS REGISTER

The 6551 continually monitors the condition of the registers and the quality of the incoming data. When I/O location C0F1 (R) is accessed the contents of the Status Register is placed on the data bus. The meanings of the eight bits of the status byte are detailed following the illustration.

C0F1 (R) STATUS REGISTER

IRQ--Bit 7 indicates that the 6551 generated an IRQ to the system for one of the folllowing conditions:

1. Change of status of the DCD line.
2.. Change of status of the DSR line.
3. The Transmit Register has emptied.
4. The Receive Register has filled with a new incoming character.

(Note: the third and fourth conditions are program controlled as to whether or not they inititate an IRQ).

DSR---Bit 6 indicated the status of the DSR line from the interface. 0=DSR is low and ready. 1=DSR is high and not ready.

DCD---Bit 5 shows the condition of the Data Carrier Detect line from the interface. 0=DCD is low and the carrier is detected. 1=DCD is high and not ready.

TDRO--Bit 4 informs the host that the Transmit Data Register has transferred its contents to the outputs shift register and now ready to accept another character (byte). 0=not empty, 1=empty.

RDRF1-Bit 3 indicates that the Received Data Register has been filled with a character from the line. 0=not full, 1=full.

OVERR-Bit 2 shows that there has been an overrun error, that is, a new character has been transferred to the Received Data Register before the previous received character was taken by the program and the RDRF1 flag reset. This error will not generate an IRQ but should be checked by the program so that tht lost data can be recovered. 0=no overrun, 1=overrun has occurred.

FRMERR-Bit 1 informs the program that the incoming data did not conform to the parameters set in the Control Register. That means usually that when the 6551 checked for the position and number of stop bits if found a descrepency. This error most often happens when the remote device is transmitting at a different baud rate. 0=no framing error, 1=framing error detected. This error does not generate an IRQ.

PARERR--Bit 0 indicates that there has been a parity error in the incoming data. This error does not cause an IRQ to be generated. 0=no parity error,1=parity error detected.

## PROGRAMMED RESET

By accessing COF1 (w) the Status Register will be reset to all 0's. The data byte on the bus at that cycle does not have to be any particular structure.

COF1 (w) PROGRAMMED RESET (w)

## COMMAND REGISTER

To access the Command Register to initialize or modify the Command byte a COF2 (w) must be executed with the data byte configured for the desired effect. To inspect the contents (or current command structure) a COF2 (R) will cause the 6551 to place the contents of the Command Register on the data bus. The meaning of each bit is explained below.

COF2 (r/w) COMMAND REGISTER (r/w)

Parity ck ctrls--Bits 7 through 5 command the 6551 in regard to parity checking. Bit 5 is parity enable. Bit 7 determines whether the parity bit position will have odd/even or fixed one/zero function. Bit 6, depending on the condition of Bit 7 selects either odd or even parity, or fixed mark (one) or fixed zero (space). Table -- below clearly shows the conditions of these bits.

ECHO--Bit 4 determines whether the 6551 will echo (transmit a duplicate image of what is received) the received data to the remote device. 0=no echo, 1=echo data.

TRANS CTRLS--Bits 3 and 2 control the 6551 in three (3) functions. They are Transmit Interrupt, the state of the RTS line, and the Transmit BRK (break, a continuous space on the line for approximately 200 milliseconds). Table -- shows which state controls which function.

INT--Bit 1 command the 6551 to either enable or disable interrupt on Received Data Register full (bit 3 of the status byte). 0=IRQ on RDRF1, 1=no interrupt.

DTR--Bit 0 enable the 6551 to transmit and receive or not. It also changes the state of the DTR output to match the condition of the 6551. 0=disable xmit/rcv (DTR high), 1=enable Xmit/Rcv (DTR low).

## CONTROL REGISTER

The final I/O location on the 6551 is the Control Register. By writing to CPF3 (w) with a properly structured date byte four functions are controlled. They are Number of Stop bits appended to outgoing data byte (and checked for on the incoming date byte), the source of the receiver clock, and the baud rate selection. By reading location COF3 (x) the current control configuration can be seen on the data bus.

COF3 (R/W) CONTROL REGISTER (R/W)

STOPB--Bit 7 controls the number of stop bits that will be added to the transmitted data word. 0=1stop bit, and depending on the word length selection 1=2 stop bits or 1 bit if word length is 8 and parity is selected, or 1/2 bits if word length is 5 and no parity is selected.

WORD LEN--Bits 6 and 5 determine the number of data bits that will be transmitted or received in the data word. The values (6,5) are as follows: 0,1=7 bits; 1,0=6 bits; 1,1=5 bits.

'XCLK--Bit 4 indicates the source of the receiver clock. 0=external clock source, 1=baud rate generator (internal). When the internal selection is made the RxC pin becomes an output.

BAUD RATE--Bits 3 through 0 select the baud rate at which the 6551 will operate. Table -- details the various selections available based on a standard 1.8432 MHZ clock input. It should be noted that 0,0,0,0 selects the external clock as the baud rate source but the clock rate is actually dividied by 16 so the external clock should be 16x the desired baud rate.

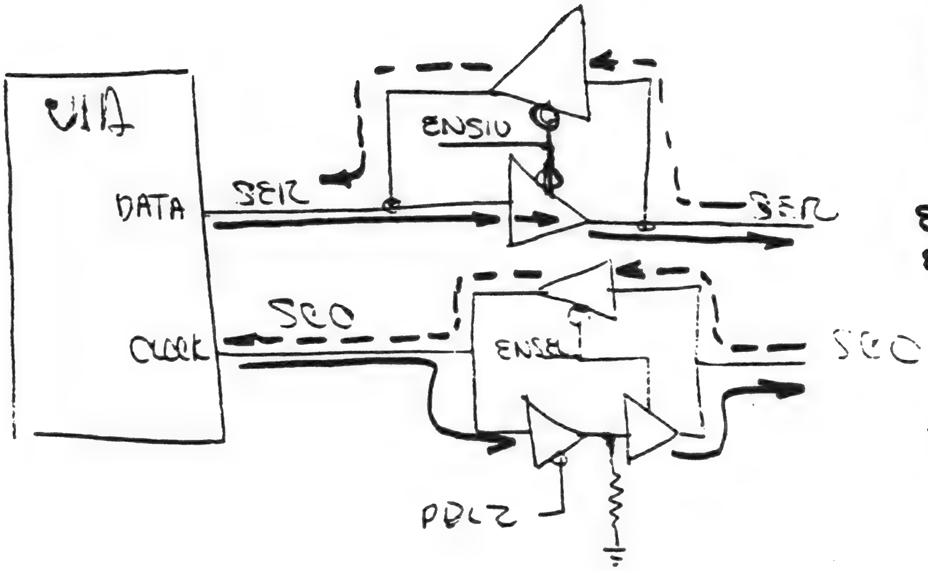
## SIMPLE SERIAL PORT

Incorporated into the A /// logic design is a provision for a simple serial port. Its main purpose is to support a Silentype printer. However, it is not a dedicated port since it shares the same connector with one of the joysticks. The user has the option of having the Silentype or a second joystick. For most applications, one joystick is more than enough since the A /// is not really intended for a "games" player. The joystick would be used more for applications like cursor control.

The serial port is actually derived from a feature of the VIA. Two of the port control lines (PB1, PB2) can be configured to be a shift register, hence a simple serial port (see the section on VIA's and read the spec sheet in the appendices). In the system certain other software controlled switches must be set to enable the port. These switches are found in another addressable latch (U177). They control the direction of data and clock to and from the board. The VIA is programmed internally to determine its function.

The signal ENSIO when high enables data from the VIA to the port, when low it enables data from the port to the VIA. The signal ENSEL determines the direction of the clock, high enables clock from the VIA to the port (if and only if PDL2 is low), low enables the port to supply the clock to the VIA. ENSEL when high also enables the AXCO signal to the port, this can be used as a select or acknowlege to the remote device. The remote device may put status bits on the "switch" line which can be used to notify the processor of some requirement mutually agreed upon.

# — SIMPLE SERIAL PORT —


VIA
DATA
SER
ENSIO
SER
CLOCK
SCO
ENSEL
SCO
PDLZ

DATA

ENSIO=1 = OUT
ENSIO=0 = IN

CLOCK

ENSEL=1= OUT*
ENSEL=0= IN

* IF PDLZ=0
IF PDLZ=1
THE OUTPUT ..
HELD LO.

NOTE: THE VIA MAY SEND DATA USING IT'S OWN CLOCK OR IT MAY BE SHIFTED WITH A REMOTE CLOCK.

ALSO IT MAY STROBE DATA IN WITH IT'S OWN CLOCK OR IT MAY BE STROBED IN WITH A REMOTE CLOCK

## PINOUT OF THE RS-232-C SERIAL INTERFACE (PORT C)

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | SGND | Shield GrouND. |
| 2 | TXD | Transmitted Data; serial data output from the Apple. |
| 3 | RCD | ReCieved Data; serial input to the Apple. |
| 4 | RTS | Request To Send output; this indicates that the Apple is ready to transmit data. This line is active whenever the Serial Card emulation is used. |
| 5 | CTS | Clear To Send input; this acknowledges that the Apple may begin transmission. This line is ignored by the Serial Card emulation. |
| 6 | DSR | Data Set Ready input; this acknowledges that the remote device is operational. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This can be used to prevent the Apple from overflowing a printer input buffer. |
| 7 | GND | Signal GrouND. |
| 8 | DCD | Data Carrier Detect; this acknowledges that the remote device is ready to transmit data. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This line can be used to prevent the Apple from overflowing a printer input buffer. |
| 9-19 | | No connect. |
| 20 | DTR | Data Terminal Ready output; this indicates that the Apple is on and operational. This line will be active anytime the Serial Card emulation is used. |

## THE ACIA

The Apple /// has a built-in 6551 ACIA (Asynchronous Communication Interface Adapter). It is located at addresses $C0F0 thru $C0F3 (decimal -16144 to -16141). The ACIA has five registers: transmit data, receive data, status, command, and control.

The transmit register ($C0F0) is used to send data out the Apple /// to an external device, such as a modem or a printer. A byte is transmitted by setting the control and command registers appropriately and then polling the status register. When bit 4 of this register is one the ACIA is ready to shift the next byte out. Often bits 5 and 6 are tested for zero to assure the Data Carrier Detect and Data Set Ready are valid as some printers use these lines as handshake signals.

Care must be taken when writing to the transmit data register as it is at the same address as the receive data register. The 6502 will do false reads when certain address modes are used, thus discarding whatever was in the receive data register.

The receive data register ($C0F0) contains the last byte received from an external source, such as a modem. Bit 3 of the status register is one whenever this register is full.

The status register ($C0F1) indicates the states of Data Set Ready, Data Carrier Detect, whether the transmit and receive registers are full, and whether a framing, overrun or parity error has occured on input.

The command register ($C0F2) sets the parity, echo mode, transmit and receive enables, and BRK transmission.

The control register ($C0F3) sets the number of stop bits, data word length, receiver clock source, and baud rate.

### PHYSICAL PINOUT OF THE RS-232-C SERIAL INTERFACE

```
13   12   11   10   9    8    7    6    5    4    3    2    1
   25   24   23   22   21   20   19   18   17   16   15   14
```

## RS232 CONNECTOR USAGE (PORT C)

The Apple /// is classified as Data Terminal Equipment (DTE) under the EIA RS-232-C interface specification. It can be directly connected to a piece of Data Communications Equipment (DCE), such as a modem. To connect the Apple to another piece of Data Terminal Equipment (such as a printer), you must use a modem eliminator.

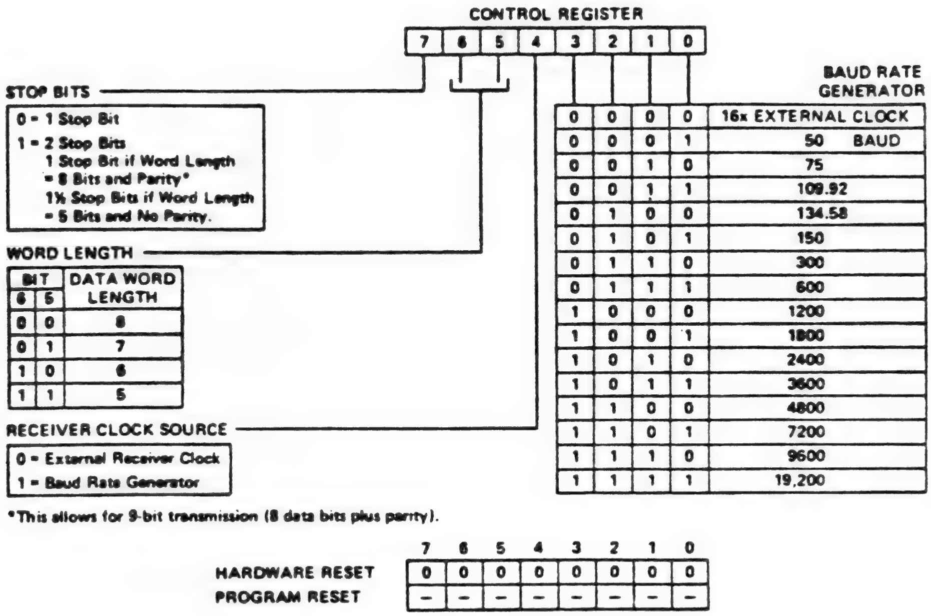
All output levels are minimum +6 volts when logic 0 and maximum -6 volts when logic 1, measured into a 3K ohm load.

All inputs have a turn-on positive going threshold of +1.25 volts and a turn-off negative going theshold of +.8 volts, typical. All inputs sink a 10 mA current, maximum.

## CONTROL REGISTER

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

C0F3


CONTROL REGISTER
7 6 5 4 3 2 1 0
STOP BITS
WORD LENGTH
RECEIVER CLOCK SOURCE
BAUD RATE GENERATOR

**STOP BITS**

0 = 1 Stop Bit

1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

**WORD LENGTH**

| BIT 6 | BIT 5 | DATA WORD LENGTH |
|---|---|---|
| 0 | 0 | 8 |
| 0 | 1 | 7 |
| 1 | 0 | 6 |
| 1 | 1 | 5 |

**RECEIVER CLOCK SOURCE**

0 = External Receiver Clock

1 = Baud Rate Generator

**BAUD RATE GENERATOR**

| 3 | 2 | 1 | 0 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 16x EXTERNAL CLOCK |
| 0 | 0 | 0 | 1 | 50 BAUD |
| 0 | 0 | 1 | 0 | 75 |
| 0 | 0 | 1 | 1 | 109.92 |
| 0 | 1 | 0 | 0 | 134.58 |
| 0 | 1 | 0 | 1 | 150 |
| 0 | 1 | 1 | 0 | 300 |
| 0 | 1 | 1 | 1 | 600 |
| 1 | 0 | 0 | 0 | 1200 |
| 1 | 0 | 0 | 1 | 1800 |
| 1 | 0 | 1 | 0 | 2400 |
| 1 | 0 | 1 | 1 | 3600 |
| 1 | 1 | 0 | 0 | 4800 |
| 1 | 1 | 0 | 1 | 7200 |
| 1 | 1 | 1 | 0 | 9600 |
| 1 | 1 | 1 | 1 | 19,200 |

*This allows for 9-bit transmission (8 data bits plus parity).

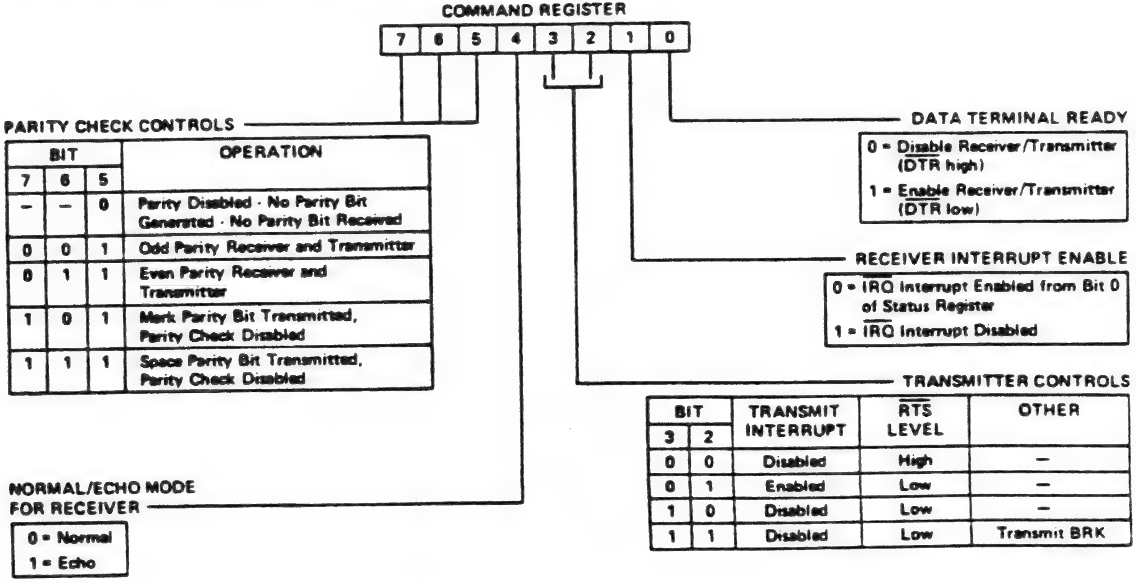
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| HARDWARE RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PROGRAM RESET | – | – | – | – | – | – | – | – |

Figure 6. Control Register Format

## COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

C0F2


COMMAND REGISTER
7 6 5 4 3 2 1 0
PARITY CHECK CONTROLS
NORMAL/ECHO MODE FOR RECEIVER
DATA TERMINAL READY
RECEIVER INTERRUPT ENABLE
TRANSMITTER CONTROLS

**PARITY CHECK CONTROLS**

| BIT 7 | BIT 6 | BIT 5 | OPERATION |
|---|---|---|---|
| – | – | 0 | Parity Disabled · No Parity Bit Generated · No Parity Bit Received |
| 0 | 0 | 1 | Odd Parity Receiver and Transmitter |
| 0 | 1 | 1 | Even Parity Receiver and Transmitter |
| 1 | 0 | 1 | Mark Parity Bit Transmitted, Parity Check Disabled |
| 1 | 1 | 1 | Space Parity Bit Transmitted, Parity Check Disabled |

**NORMAL/ECHO MODE FOR RECEIVER**

0 = Normal

1 = Echo

**DATA TERMINAL READY**

0 = Disable Receiver/Transmitter ($\overline{DTR}$ high)

1 = Enable Receiver/Transmitter ($\overline{DTR}$ low)

**RECEIVER INTERRUPT ENABLE**

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 0 of Status Register

1 = $\overline{IRQ}$ Interrupt Disabled

**TRANSMITTER CONTROLS**

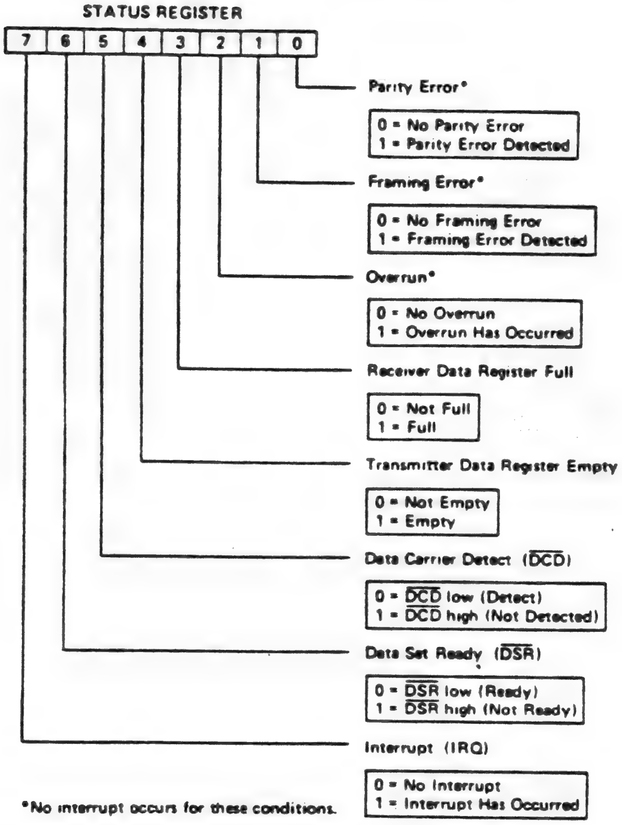
| BIT 3 | BIT 2 | TRANSMIT INTERRUPT | $\overline{RTS}$ LEVEL | OTHER |
|---|---|---|---|---|
| 0 | 0 | Disabled | High | – |
| 0 | 1 | Enabled | Low | – |
| 1 | 0 | Disabled | Low | – |
| 1 | 1 | Disabled | Low | Transmit BRK |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| HARDWARE RESET | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| PROGRAM RESET | – | – | – | 0 | 0 | 0 | 1 | 0 |

Figure 7. Command Register Format

## STATUS REGISTER C0F1

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.

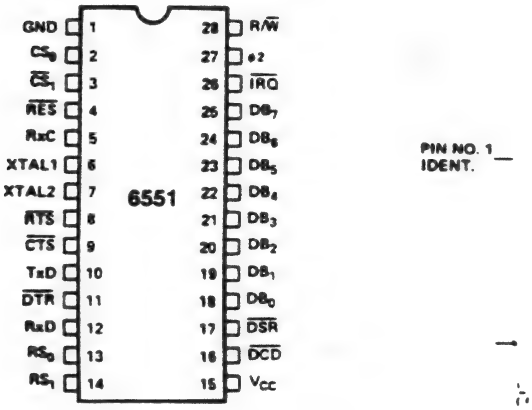

STATUS REGISTER
7
6
5
4
3
2
1
0
Parity Error*
0 = No Parity Error
1 = Parity Error Detected
Framing Error*
0 = No Framing Error
1 = Framing Error Detected
Overrun*
0 = No Overrun
1 = Overrun Has Occurred
Receiver Data Register Full
0 = Not Full
1 = Full
Transmitter Data Register Empty
0 = Not Empty
1 = Empty
Data Carrier Detect ($\overline{DCD}$)
0 = $\overline{DCD}$ low (Detect)
1 = $\overline{DCD}$ high (Not Detected)
Data Set Ready ($\overline{DSR}$)
0 = $\overline{DSR}$ low (Ready)
1 = $\overline{DSR}$ high (Not Ready)
Interrupt (IRQ)
0 = No Interrupt
1 = Interrupt Has Occurred

*No interrupt occurs for these conditions.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| HARDWARE RESET | 0 | – | – | 1 | 0 | 0 | 0 | 0 |
| PROGRAM RESET | – | – | – | – | – | 0 | – | – |

Figure 8. Status Register Format

## PIN CONFIGURATION


GND 1
$CS_0$ 2
$\overline{CS_1}$ 3
$\overline{RES}$ 4
RxC 5
XTAL1 6
XTAL2 7
$\overline{RTS}$ 8
$\overline{CTS}$ 9
TxD 10
$\overline{DTR}$ 11
RxD 12
$RS_0$ 13
$RS_1$ 14
6551
28 R/$\overline{W}$
27 $\phi 2$
26 $\overline{IRQ}$
25 $DB_7$
24 $DB_6$
23 $DB_5$
22 $DB_4$
21 $DB_3$
20 $DB_2$
19 $DB_1$
18 $DB_0$
17 $\overline{DSR}$
16 $\overline{DCD}$
15 $V_{CC}$
PIN NO. 1 IDENT.

## SYSTEM CLOCKS & TIMING

### MAIN CLOCK (C14M)

The Apple /// has as its master clock a 14 megahertz crystal controlled oscillator. The active components of the clock circuitry are Q10, Q11, and Y1. The exact frequency of the oscillator is 14.318 MHz. The slight increase over 14 MHz is compensated for in other logic. Device B13 provides buffering and power amplification to drive all the other loads on the C14M and C14M* lines.

### FREQUENCY DIVIDER

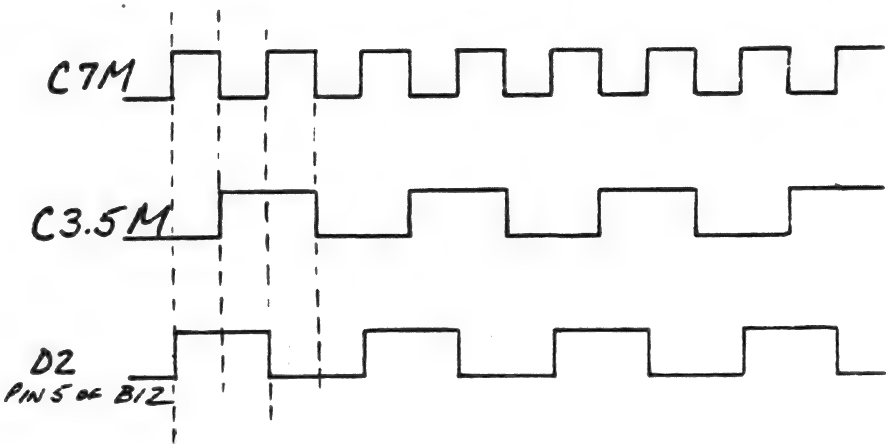
The next circuit in the system clock section is the frequency divider formed by device B12 and B13. This develops both the C7M* and the C3.5M*.

The C7M signal is developed by clocking the Q* output into the data input of a D-type latch. This results in a divide-by-two function of the clock frequency.

The C3.5M clock is developed in the same manner. However, the data input to the latch is an Exclusive-Or function of C7M and C3.5M at B13. This accomplishes two functions:

- it divides the C14M clock by 4, and
- it gives a definite phase relationship of C7M to C3.5M clocks.

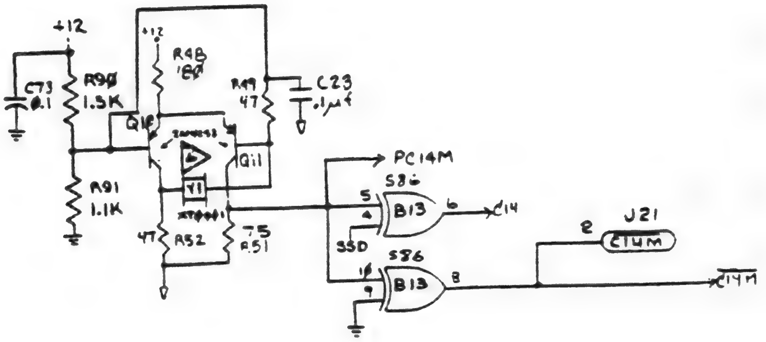
Looking at the timing diagram below we see that the D2 input of B12 is high if either the C7M or the C3.5 clock is high but not when both are high. This function is effectively at 3.5 MHz which toggles on the positive edge of the 7MHz clock. The true C3.5M signal toggles on the negative edge of the C7M clock.



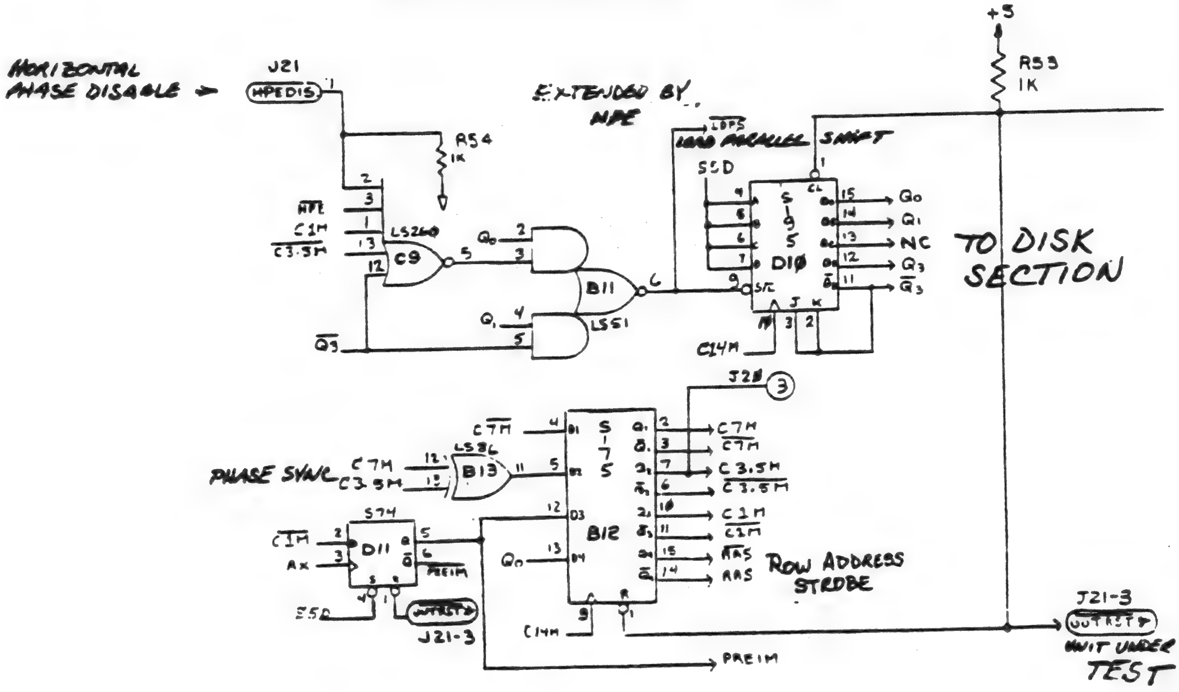
### "Q" TIMING

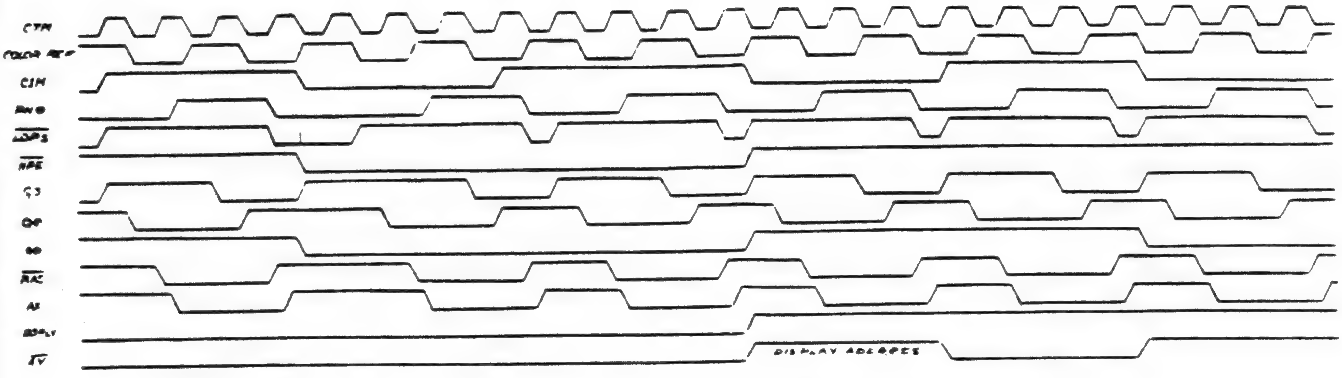
The Q clocks are a series of 2 MHz clocks which are out of phase with one another by one clock time (refer to the Apple /// Timing diagrams). The rest of the system timing depends on the states of the "Q" outputs. They provide the basis

## MAIN CLOCK - 14MHz

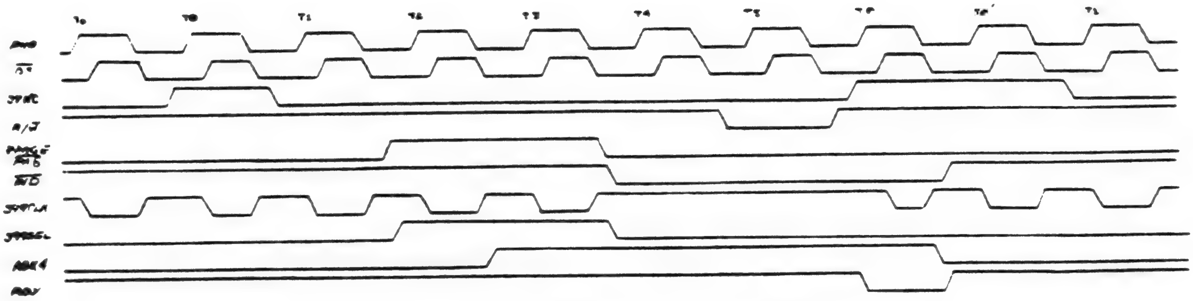

+12
C73
0.1
R90
1.5K
R91
1.1K
+12
R48
180
R49
47
C23
.1μf
Q10
2N4258
Q11
Y1
XT0001
47
R52
75
R51
PC14M
S86
5
4
B13
6
C14
SSD
S86
10
9
B13
8
2
J21
C14M
C14M

## FREQUENCY DIVIDER.

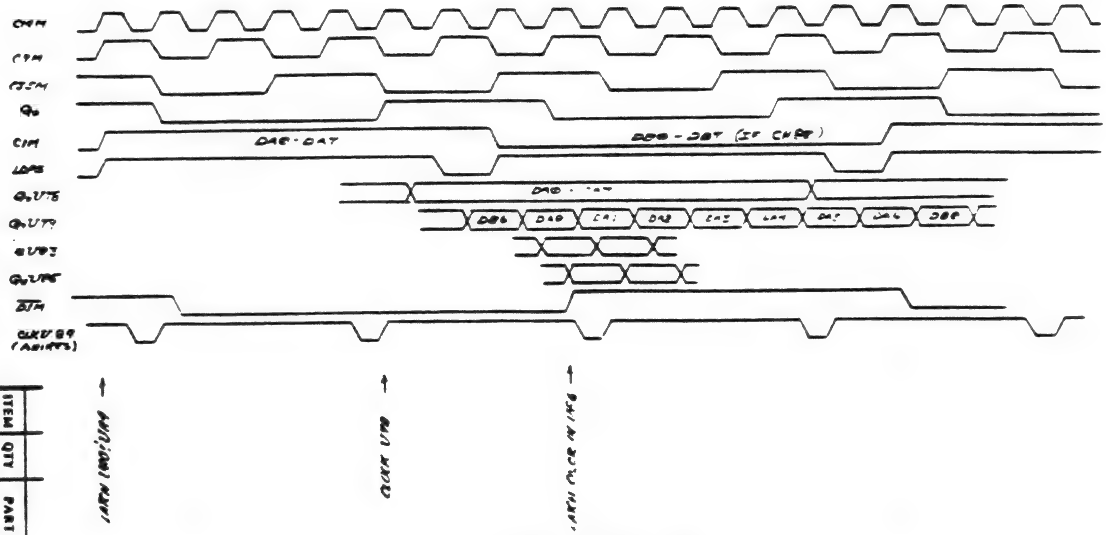

+5
R53
1K
HORIZONTAL PHASE DISABLE →
J21
HPEDIS
1
R54
1K
EXTENDED BY HPE
LDPS
LOAD PARALLEL SHIFT
SSD
2
3
HPE
1
C1M
13
C3.5M
12
LS260
C9
5
Q0
2
3
B11
6
Q1
4
5
LS51
Q3
S
9
5
D10
CL
S/L
J
K
4
5
6
7
9
1
15
14
13
12
11
3
2
C14M
Q0
Q1
NC
Q3
Q3
TO DISK SECTION
J20
3
C7M
4
D1
S
1
7
5
Q1
Q1
Q2
Q2
Q3
Q3
Q4
Q4
2
3
7
6
10
11
15
14
C7M
C7M
C3.5M
C3.5M
C1M
C1M
RAS
RAS
ROW ADDRESS STROBE
PHASE SYNC
C7M
C3.5M
12
13
LS86
B13
11
5
D2
12
D3
B12
Q0
13
D4
S74
C1M
2
AX
3
D11
Q
Q
5
6
PREIM
S
R
4
1
SSD
OUTRST
J21-3
C14M
9
R
1
PREIM
J21-3
OUTRST
UNIT UNDER TEST


CTM
COLOR REF
C1M
RAS
LDPS
NPE
Q3
AX
RAS
DSPLY
DISPLAY ADDRESS

EXTRA NPE CYCLE & DISPLAY TIMING


T0
T0
T1
T2
T3
T4
T5
T0
T0'
T1
SYNC
R/J
PAGE
RDY

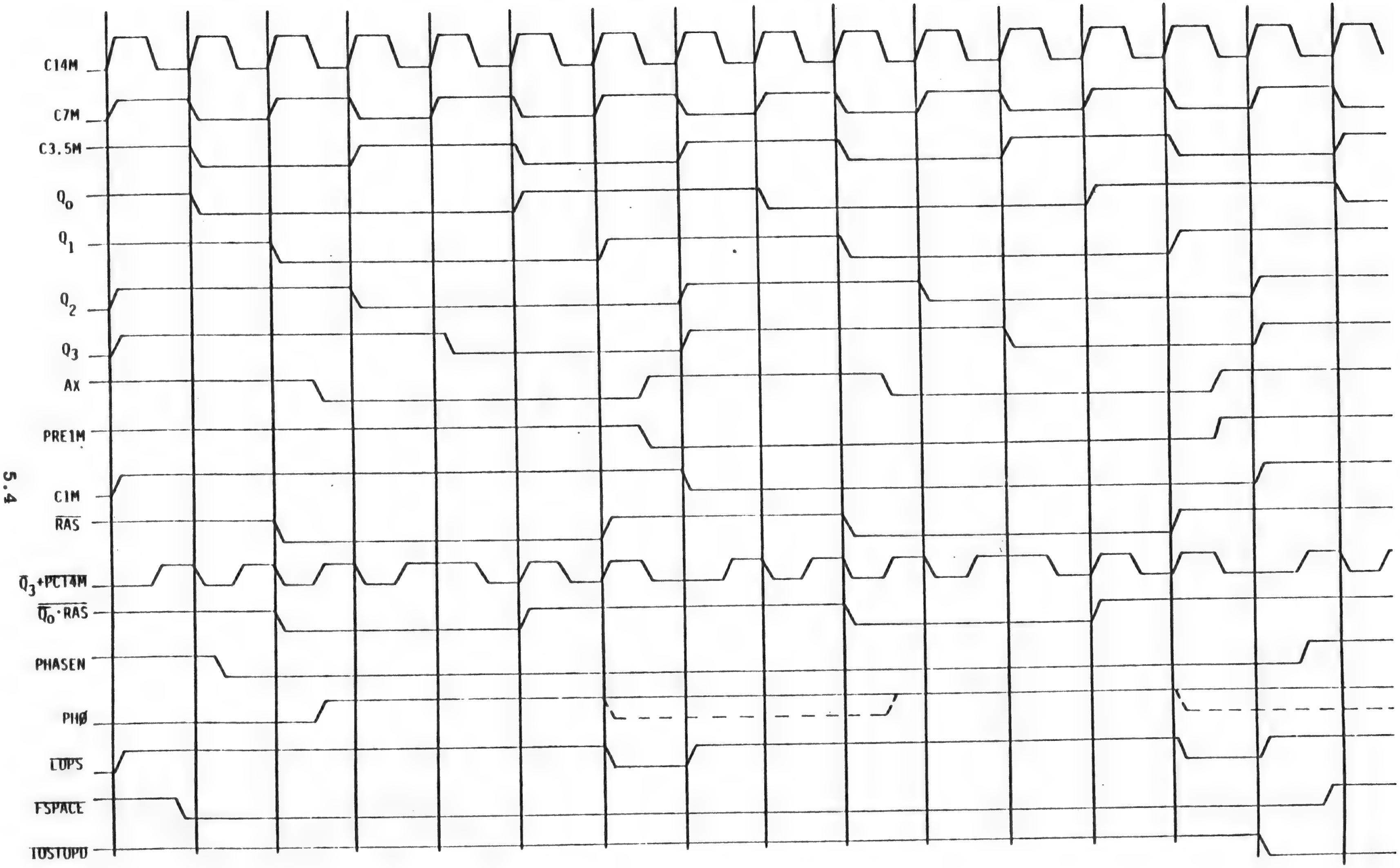
INDIRECT ADDRESS TIMING


C7M
C3.5M
C1M
LDPS
DA0 - DA7
DB0 - DB7 (IF CHR)
DB6
DB0
DA0
DA2
DA4
DA6
DB0
DTM

VIDEO SIGNALS

# A /// SYSTEM TIMING

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING
NEXT ASSY
FINISH
MATERIAL
TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DECIMALS .X ±
.XX ±
.XXX ±
ANGLES ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS
ITEM QTY PART NUMBER DESCRIPTION
DRAWN BY DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE
apple computer
TITLE
SIZE C
DRAWING NUMBER
SCALE
SHEET


C14M
C7M
C3.5M
$Q_0$
$Q_1$
$Q_2$
$Q_3$
AX
PRE1M
C1M
$\overline{RAS}$
$\overline{Q}_3$+PC14M
$\overline{\overline{Q}_0 \cdot RAS}$
PHASEN
PHØ
$\overline{LDPS}$
$\overline{FSPACE}$
$\overline{IOSTOPD}$

APPLE III TIMING

for processor and RAM address timing.

The Q clocks are initialized with each Load Parallel to Serial pulse (LDPS), which changes the mode of the LS195 (D10) from a shift register to a parallel loaded register when low. At each load, all of the bits are set high. When LDPS* returns high the next clock will shift the zero of Q3* across the register. This means that Q0 will stay high for one clock cycle. Q1 will stay high for 2 clocks, etc. When the Q3* goes high at the forth clock edge after LDPS the JK input will now see a "1". Subsequent clocks will start shifting that one across the register. When Q1 goes high again, LDPS* will be enabled low and another load will be accomplished at the next clock edge. The waveforms are assymmetrical. Each of Q0-Q2 are up for three clocks and down for four. Q3 is up for four and down for three.

This type of cycling will continue for 128 cycles. Then the Horizontal Phase Disable (HPE*) "freeze" will occur.

## HPE* FREEZE

The HPE* signal will cause the Q states to extend their next cycle by two clock times. The purpose of the shift is to shift the phase of the color reference signals to the data in the video generator. A detailed discussion of this phenomenon is described in the video generator section. How this shift occurs is discussed below.

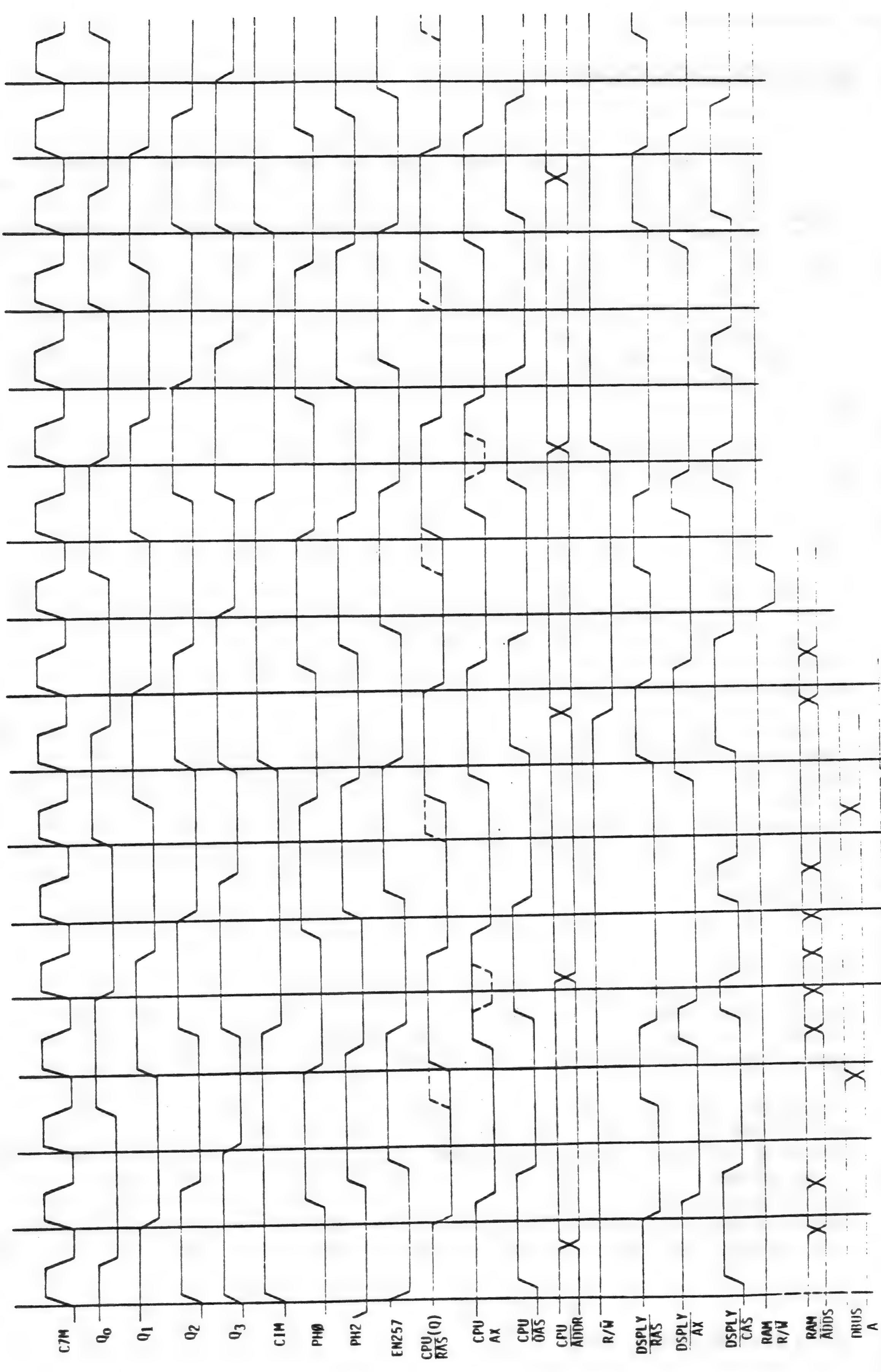
Looking at the gate array of C9 and B11 we see that since HPE* is normally high, the output of C9 is normally low. This de-gates the And inut shared with Q0, and allows LDPS to function as usual. But when HPE* goes low, which will always coincide with C14M going low, the And gate shared with Q0 will become enabled and cause the extension of the LDPS* for two extra clock cycles. This state will exist until C3.5M returns high and relieves LDPS*. The next clock will change the state of Q0 and that will not be able to "disrupt" the clocks until the next HPE pulse.

## AX, PRE1M, & C1M

The AX, RAM address (the signal used to select which addressing source [row or column] is presented to the RAMs: see RAM Address Logic) is another 2 Mhz signal which lags Q1 by one half clock cycles. It is developed at A11 pin 9.

PRE1M can toggle at each positive edge of AX, if the data input to the latch is at the opposite state. Looking at D11 (C1M*) we will be able to see just that. If PRE1M has just toggled low, one half clock cycle later C1M* will toggle high which forms the data input to the PRE1M Flip-Flop. But remember, the clock to the flip-flop is AX, a 2 MHz signal. D11 pin 5 acts much like B12 pin 2 in that the data is always opposite to the "Q" output of the latch at the time of the clock edge, therefore we have a "clock divided by 2" function, of a 1 MHZ output.

## RAS (Row Address Strobe)


C7M
Q0
Q1
Q2
Q3
C1M
PH0
PH2
EN257
CPU RAS(Q)
CPU AX
CPU OAS
CPU ADDR
R/W
DSPLY RAS
DSPLY AX
DSPLY CAS
RAM R/W
RAM ADDS
DBUS A
DBUS B

The RAS signal is Q0 delayed by one clock and inverted. This is acccomplished at D10 pin 15 & 14. (Note: the inversion is done by calling the "Q" output the active low signal RAS*, clever huh?) RAS is used in the RAM address logic to develop the "row select" signals for the RAMs.

## VIDEO HORIZONTAL & VERTICAL STATE COUNTERS

This circuit is made up of four 4-bit binary counters, (F10, F11, G11, G12), which develop the essential signals for partitioning the screen and addressing the RAM for all the video data.

Basically, there are two sections of the circuit:

1 - horizontal postion counter

2- vertical position counter

These two counters form the X and Y coordinates of each addressable byte on the screen. Each byte contains 7 bits or dots in 40 character modes.

From the various discussions about the Apple ///, we have learned that in the 40 character mode there are 280 dots across the horizontal line that can be defined, and 192 of these horizontal line (280 X 192). In the Apple /// modes there are 560 dots in the horizontal line, however, there are still only 192 horizontal lines (560 X 192).

The Video Counter works identically in either of these modes. It provides the resolution of 40 by 192 matrix. Each one of the 40 horizontal positions defines either 7 or 14 dots (40 or 80 character modes, respectively). These dots are actually bits of data bytes in memory that are parallel loadedd into a shift register and shifted out serially to the video monitor. In the 40 character modes the system loads the shift register at a 1 MHz rate and shifts at a 7 MHz rate. In the 80 character modes it loads at a 2 MHz rate and shifts at a 14 Mhz rate. It is interesting to note that in either mode the state counter increments at a 1 Mhz rate.

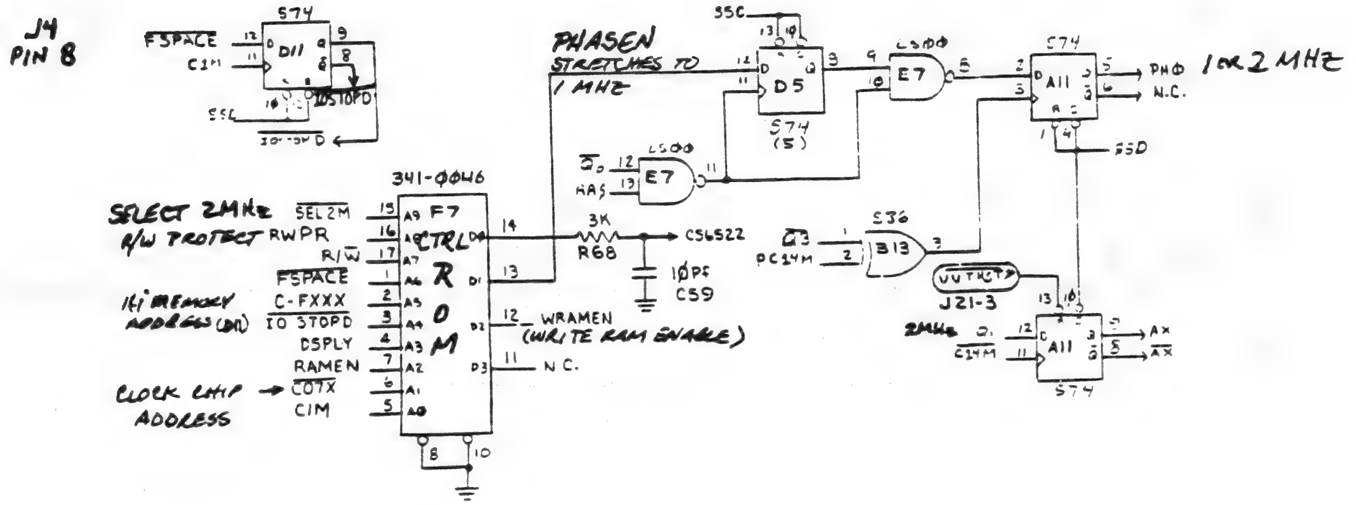
The system provides two complete accesses for the video output per increment of the state counter, but in the 40 character modes one of these are masked out.

## HORIZONTAL SECTION

The Horizontal section of the state counter uses 7 of the counter stages and develops the H0 through H5 and the HPE* signals. The remaining 9 stages of the counter develop the Vertical states VA, VB, VC, and V0 through V5.

The Horizontal section provides the capability of a 128 state counter, however, it only provides 65 states. This is due to the action of the most significant stage, HPE*. The counter actually counts from 64 to 128 then resets to count 64. Simply, HPE* starts high and when the counter increments HPE* low after 64 counts it is then reset to state 64 after the next clock input, this yields

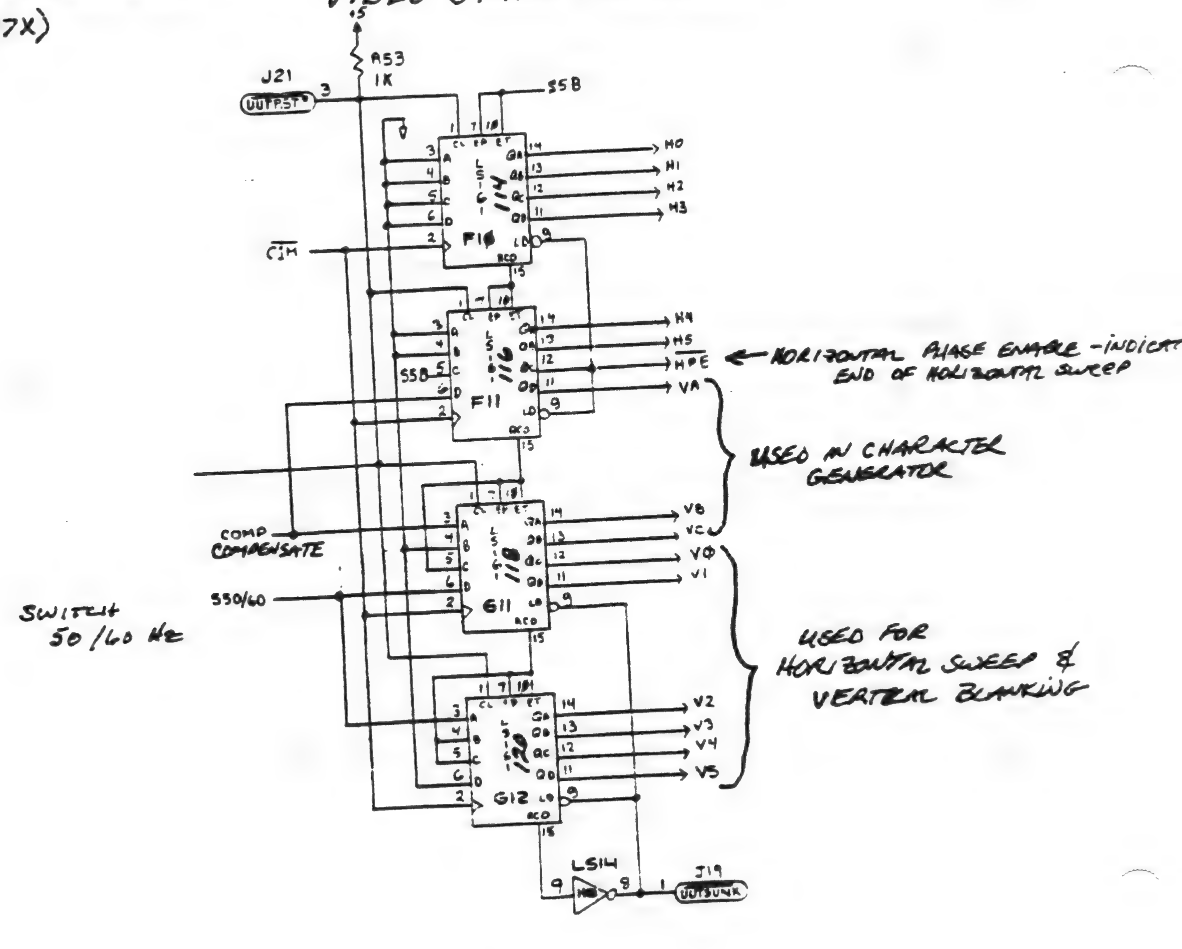
# 1 TO 2 MHz GEARSHIFT



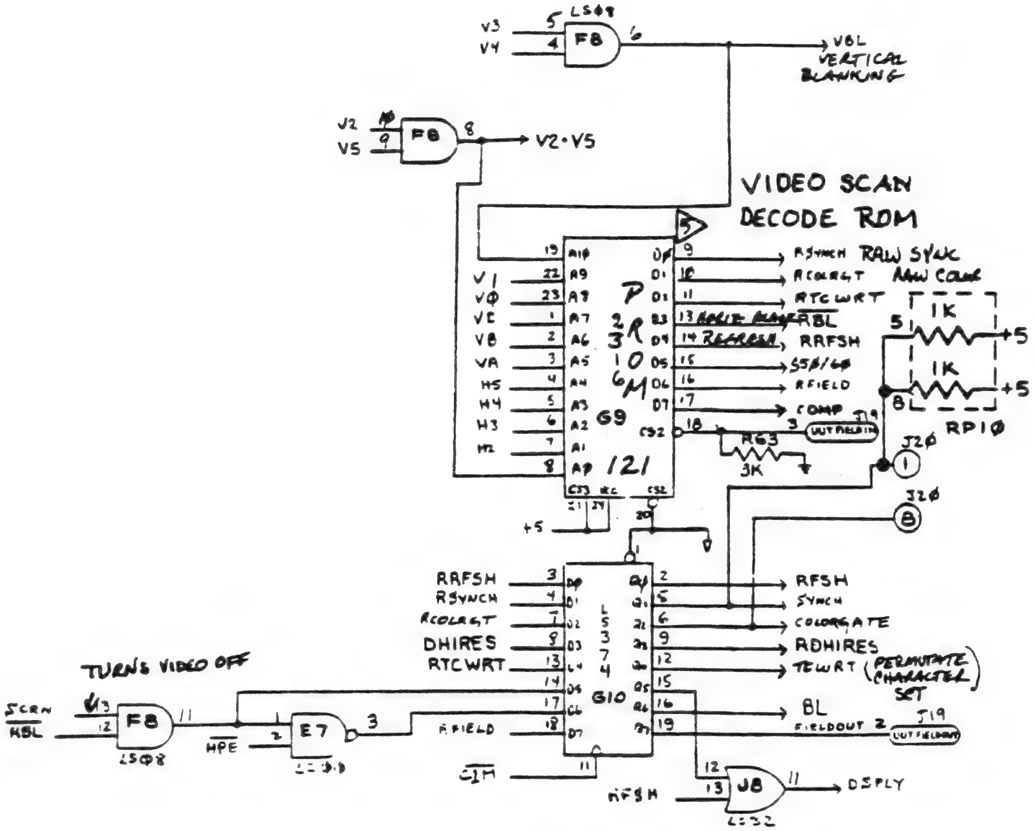
J4
PIN 8
S74
FSPACE
C1M
D11
IO STOPD
SSC
IO STOPD
PHASEN
STRETCHES TO
1 MHZ
SSC
D5
S74
(5)
LS00
E7
S74
A11
PHΦ
N.C.
1 OR 2 MHZ
SSD
Q3
RAS
LS00
E7
341-0046
F7
CTRL
R
O
M
SELECT 2MHz
SEL2M
R/W PROTECT RWPR
R/W
FSPACE
Hi MEMORY ADDRESS (D11)
C-FXXX
IO STOPD
DSPLY
RAMEN
CLOCK CHIP ADDRESS
C07X
C1M
3K
R68
CS6522
10PF
C59
WRAMEN
(WRITE RAM ENABLE)
N.C.
S36
B13
PC14M
VVTRST
J21-3
2MHz
C14M
A11
S74
AX
AX

*FSPACE* – RESULTS WHEN YOU ADDRESS THE VIA'S, THE ACIA, OR THE INTERNAL CLOCK (C07X)

# VIDEO STATE COUNTER



+5
R53
1K
J21
VVTRST
S5B
F10
LS161
C1M
H0
H1
H2
H3
F11
LS161
S5B
H4
H5
HPE
VA
← HORIZONTAL PHASE ENABLE – INDICATES END OF HORIZONTAL SWEEP
USED IN CHARACTER GENERATOR
COMP
COMPENSATE
G11
LS161
VB
VC
VΦ
V1
SWITCH 50/60 Hz
S50/60
USED FOR HORIZONTAL SWEEP & VERTICAL BLANKING
G12
LS161
V2
V3
V4
V5
LS14
J19
VVTSYNC


LS08
F8
V3
V4
VBL
VERTICAL BLANKING
V2
V5
V2·V5
VIDEO SCAN DECODE ROM
V1
V0
VC
VB
VA
H5
H4
H3
H2
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
P 3R 10 6M
G9
/121
D0
D1
D2
D3
D4
D5
D6
D7
CS2
CS3
VCC
+5
RSYNCH
RAW SYNC
RCOLRGT
RAW COLOR
RTCWRT
RBL
RRFSH
55/60
RFIELD
COMP
J19
OUTFIELDIN
R63
3K
1K
1K
+5
+5
RP10
J20
RRFSH
RSYNCH
RCOLRGT
DHIRES
RTCWRT
LS374
G10
RFSH
SYNCH
COLORGATE
RDHIRES
TCWRT
(PERMUTATE CHARACTER SET)
BL
FIELDOUT
OUTFIELDOUT
TURNS VIDEO OFF
SCRN
HBL
HPE
E7
RFIELD
C1M
RFSH
J8
LS32
DSPLY

65 states all together.

Looking at F11 we see that the HPE* output is connected to the "load" input of F10 and F11. At the next clock input these two devices will be loaded with the state determined by what is on the data inputs. All inputs except pin 5 of F11 are tied low (disregard the input to pin 6 of F11 at this time). This binary state equals 64. So rather than starting back at "zero" the counter jumps to 64.

For real time considerations of the monitor, it takes 25 states or 25 microseconds for the sweep to return from the right hand side to the left side. So the system ignores the first 25 states and blanks the video output and the returning trace is not shown. The boolean expression for the horizontal blanking would be expressed:

(H4* and H5*) or (H4 and H3*)

This logical function is done within the G9 Control ROM. Refer to page 10 of 10 of the schematic diagram.

In summary, the horizontal counter provides the address necessary for the display. It divides the horizontal line into forty (40) sections, and yields the timing for horizontal blanking. The HPE* signal is used to momentarily "freeze" some of the system timing.

## VERTICAL SECTION

The Vertical State Counter provides the Y-axis of the display matrix. The nine stages, if left alone to count, would provide 512 states. As in the horizontal counter, it is preset to count higher than zero eadch time it reaches the "terminal count". Also, some of the states are used to blank the video while the trace returns from the bottom of the screen to the top (VBL).

The vertical counter effectively counts the number of HPE*'s that have occurred, or simply, the number of horizontal lines that have been generated in this scan.

At this time the counter is reset to count 250. Look at the timing diagram of the vertical counter. One can see that all vertical signals would normally go low, but instead the counter is loaded with the data inputs. VA will not be affected by the teminal count/load and will continue as discussed before. VB will be loaded to the present state of "comp" (or VA) which is high. VC and V5 will be loaded to a low and the rest of the bit states wil be loaded to "1". This will decode to decimal 250.

Six counts later VA through V4 will toggle low and V5 will toggle high. This is the point where the logic assumes to be at scan line "zero". It will now take 256 counts to reach the terminal count sequence and start again. Using some math we see that the counter defines 262 states (256+6 = 262).

Vertical blanking takes 70 of the 262 states developed by the counter. The boolean expresssion for the vertical blanking signal would be:

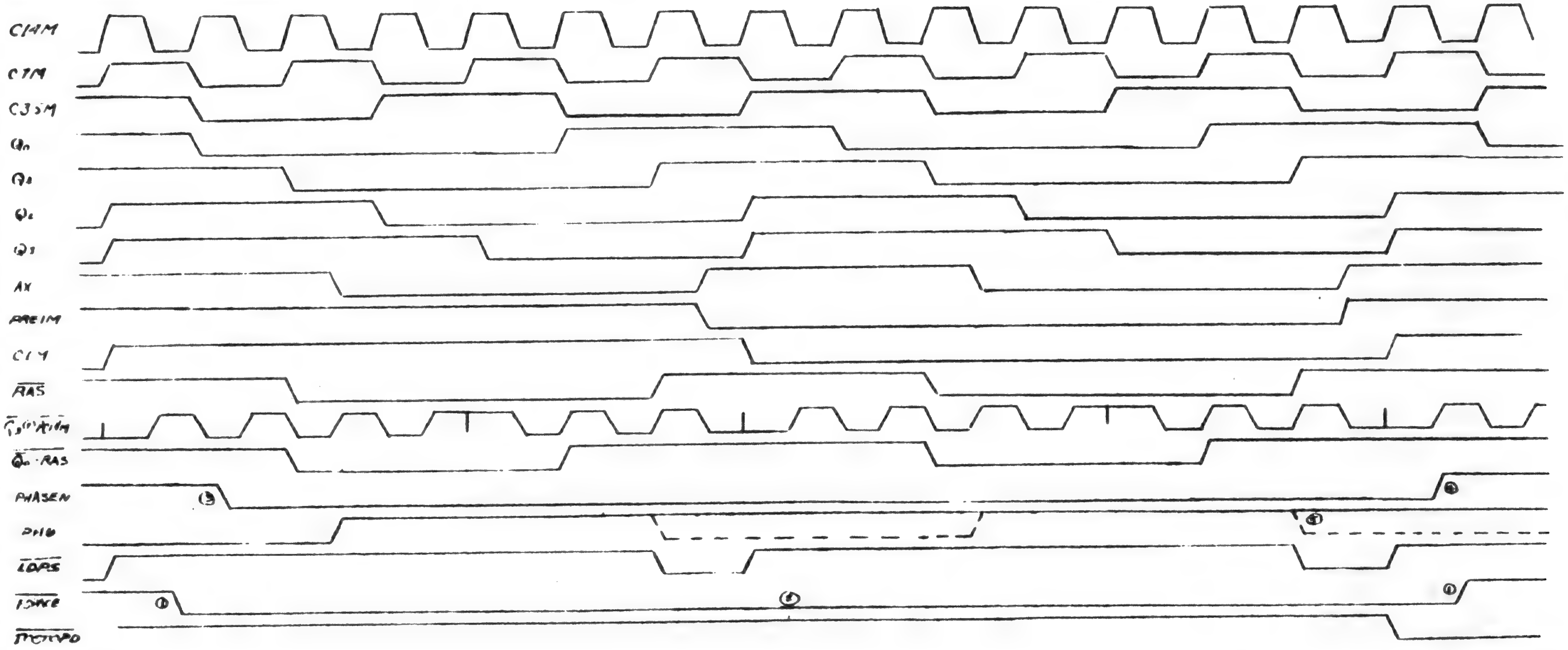
(V3 and V4)

This signal is developed at F8 pin 6 and is used in the system to indicate that a complete scan of the current display page has occurred. It is also an input to the Control Rom, G9, and therefore is a modifier to its outputs.

We were looking for the majic number of 192. Well, if you´ve been keeping track, it´s simply the difference of 272-70.

| REV. | ZONE | ECO # | REVISION |
|---|---|---|---|

**NOTE:** UNLESS OTHERWISE SPECIFIED


C14M
C7M
C3.5M
Q0
Q1
Q2
Q3
AX
PRE14M
C1M
RAS
Q3·C14M
Q0·RAS
PHASEN
PHI0
LDPS
FSYNC
TSTCPD
③
⑥
④
①
⑤
①

(1) ADDRESS TIME FROM PHØ
(2) FSYNC MAINTAINED BY PHØ STRETCH
(3) PHASEN CASE: BEGIN TSTCPD FSYNC
(4) PHASEN GOES HIGH DUE TO TSTCPD
(5) PHØ HELD HIGH ANOTHER CYCLE
TO SYNCH 6522 3 TO C1M

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

# APPLE /// SYSTEM TIMING

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES .XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS
ARE IN MILLIMETERS

| | |
|---|---|
| DRAWN BY | DATE |
| CHECKED BY | DATE |
| APPROVED BY | DATE |
| RELEASED BY | DATE |

apple compu

TITLE
APPLE /// TIMI

MATERIAL:
FINISH:
NEXT ASSY

SIZE B
DRAWING NUMB
SCALE
SHEET

# DISPLAY MODES

- 40 CHARACTER APPLE II : 40x24 CHARACTER B/W TEXT (2K BYTES RAM)
- 40 CHARACTER APPLE ///: 40x24 CHARACTER COLOR TEXT - 16 BACKGROUND, 16 TEXT COLORS
- 80 CHARACTER BLACK & WHITE APPLE ///: 80x24 CHARACTER B/W TEXT
- BLACK & WHITE HIRES: 280x192 B/W HIRES (8K RAM)
- MEDIUM RESOLUTION 16 COLOR GRAPHICS APPLE ///: 280x192 16 COLOR HIRES WITH 40x192 BACKGROUND/FOREGROUND RESOLUTION
- SUPER HIRES APPLE ///: 560x192 B/W HIRES
- APPLE /// HIRES: 140x192 16-COLOR HIRES
- RAM CHARACTER GENERATOR (128 CHARACTER)

# APPLE /// VIDEO

## INTRODUCTION

The Apple /// has 11 defined video modes of operation. There are 5 Apple ][ modes and 6 new Apple /// modes. There are now 3 text modes and 8 graphics modes. Though the Apple /// can emulate all of the Apple ][ video modes, there are many differences in the video hardware between the Apple ][ and Apple ///, including:

- 80 column text with full upper and lower case character capability
- New color text mode
- Super high resolution black and white graphics
- 2 new color hires modes

AND

- A modifiable character set

The modifiable character set is a major new feature of the Apple ///. You can now change the character set by changing the pattern in the character generator. This is possible because of a ram, instead of a fixed rom configuration.

There are also improved video outputs. An NTSC (National Television Standards Committee) composite Black and White and color composite, plus the primary video signals, are available at the back panel for mixing into the input of a high quality RBG monitor.

The Apple ][ emulation mode has the very same video modes as the Apple ][. The Apple ///, while in its native mode, can have the following modes.

## 40 Character Apple ][

This mode is equivalent to the Apple ][ text mode. The only difference is it has upper and lower characters.

- The screen is divided into 40 horizontal columns and 24 vertical lines.
- The characters are usually white dots on a black background.
- This mode has inverse video and flashing characteristics.
- This mode has no color.

- This mode has two screen pages mapped into memory:
  - Page 1 is located at 0400-07FF
  - Page 2 is located at 0800-0BFF.

## 40 Character Apple ///

This second 40 character text mode is the most interesting and, in a way, the most powerful. This is the only color text mode. It has the same screen resolution as the Apple ][, and the same video attributes. BUT it also has the ability to select both the color of the foreground (dots) and the color of the background. Sixteen (16) colors are available as in the Apple ][ Lores Graphics.

- The color resolution can be selected for each character and can change for each character.
- It is interesting to note that by down loading a character set, a new low resolution graphics mode can be manufactured from a text mode.

The page mode is different for this mode since both pages are used at once. Why? Because the first page contains the character data and the second page contains the color information. The page 2 mode reverses the mapping, that is, the characters in page 2 are stored where the color was stored in page 1, and vice versa.

In the color byte, bits 4-7 set the foreground color and bits 0-3 set the background color. The mapping between color and character is 1:1. That is, a character located in 0409, for example, has its foreground color determined by the byte in location 0809.

In the page 1 mode the mapping is as follows:

0400-07FF contain the characters

0800-0BFF contain the color information.

In the page 2 mode:

0800-0BFF contain the characters.

0400-07FF contains the color.

## 80 Character Black & White Apple ///

This new text mode is the same as the 40 column mode with the obvious exception that it has 80 columns instead of 40. This 80 column display has full upper and lower case, and inverse video.

Unlike the 40 character mode, it does not have 2 distinct pages. It uses both pages to hold the characters.

The memory mapping for Page 1 utilizes:

0400-07FF for the primary fetch

0800-0BFF for the secondary.

In this mode, location 0400 contains the first character and 0800 contains the second. The third and the fourth characters come from locations 0401 and 0801 respectively.

In the Page 2 mode the primary fetch is from 0800-0BFF and the secondary from 0400-07FF. Therefore, the first and third characters come from 0800 and 0801 and the second and fourth come from 0400 and 0401.

## Black & White Hires

This is a new graphics mode that has a 280 by 192 resolution in Black and White only.

It has two distinct pages:

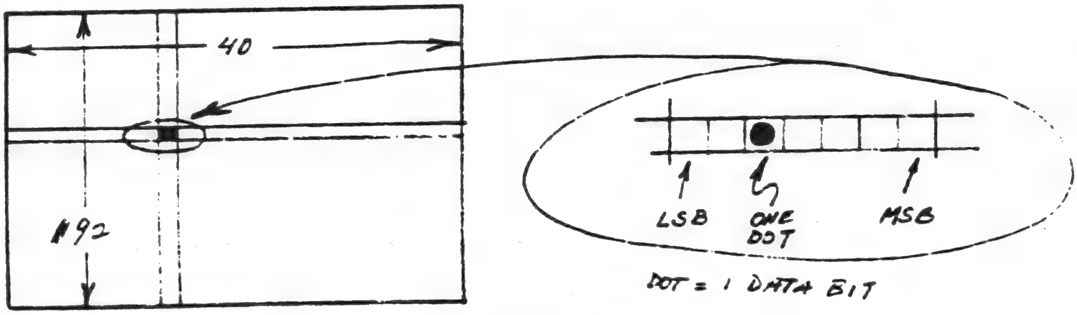
Page 1 is located at 2000-3FFF

Page 2 is located at 4000-5FFF.

## Medium Resolution 16 Color Graphics Apple ///

This is a new graphics mode for the Apple ///. It has the same dot resolution as the Apple ][ Hires (280 by 192), but it has an expanded color capability of 16 background colors. The B/W Output will yield 16 levels of grey scale.

The screen is divided into a 40 wide by 192 high matrix. That is, the color selection for foreground and 16 background can change for each 7 dot [ooooooo] pixel segment. You can think of each segment as a one-bit-high slice across a character space, as illustrated below.



The memory mapping is as follows:

| | | |
|---|---|---|
| Page 1: | 2000-3FFF | each byte represents 7 pixels in the segment |
| | 4000-5FFF | each byte represents the foreground and background colors for the corresponding 2000-3FFF byte. |
| Page 2: | 2000-3FFF | each byte represents the colors |
| | 4000-5FFF | each byte represents 7 pixels. |

## Super Hires Apple ///

This is the Apple /// Hires equivalent of 80 character mode. It is a Black and White mode which has the dot resolution of 560 Horizontal by 192 vertical spaces.

There are two distinct screen pages, each with a primary and secondary page. Because it is like the 80 character modes, this mode draws its information from alternating ram. Each memory byte contributes 7 pixels. In Page 1 mode, the primary contains the odd dot groups and the secondary contains the even dot groups. The primary (first 7 pixels) is located at 2000-3FFF, and the secondary (second 7 pixels) is found at 4000-5FFF. In Page 2 the primary is at 6000-7FFF, and the secondary is 8000-9FFF.

In each byte the Most Significant Bit (MSB) is ignored and the data is displayed with the Least Significant Bit (LSB) first from left to right.

## Apple /// Hires

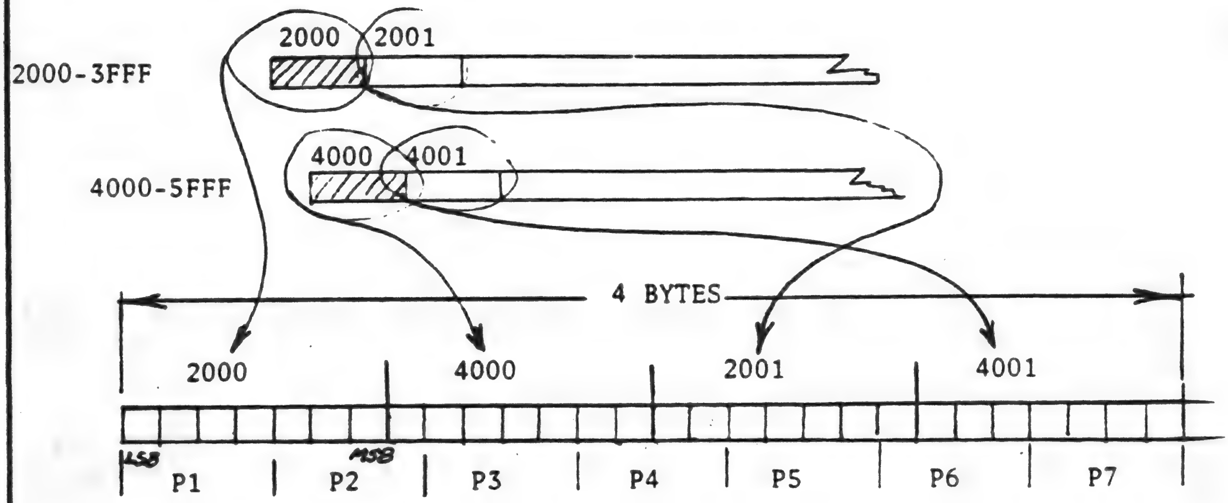
This is the third new graphics mode. It has 140 by 192 pixel resolution, and 1 of 16 color selection per pixel. In this mode the pixel is formed by a group of four dots of the same color.

There are two distinct screen pages in this mode but the mapping of the individual pages is, at first encounter, a bit difficult to master. Good luck!

- The display dot represents a sequence of 4 data bits in the RAM display area.
- Two rams are used starting at 2000 and 4000 respectively and alternate bytes are fetched from each ram area.

- In any video mode only 7 of the 8 bits of each byte are displayed.

With this information in mind...and remembering that each pixel in this mode is made from 4 bits...you can see that you need 4 bytes of information to get 7 pixels. The way in which these bytes map into picture elements is shown below.


2000
2001
2000-3FFF
4000
4001
4000-5FFF
4 BYTES
2000
4000
2001
4001
LSB
MSB
P1
P2
P3
P4
P5
P6
P7

4000-5FFF each byte represents 7 pixels.

## Super Hires Apple ///

This is the Apple /// Hires equivalent of 80 character mode. It is a Black and White mode which has the dot resolution of 560 Horizontal by 192 vertical spaces.

There are two distinct screen pages, each with a primary and secondary page. Because it is like the 80 character modes, this mode draws its information from alternating ram. Each memory byte contributes 7 pixels. In Page 1 mode, the primary contains the odd dot groups and the secondary contains the even dot groups. The primary (first 7 pixels) is located at 2000-3FFF, and the secondary (second 7 pixels) is found at 4000-5FFF. In Page 2 the primary is at 6000-7FFF, and the secondary is 8000-9FFF.

In each byte the Most Significant Bit (MSB) is ignored and the data is displayed with the Least Significant Bit (LSB) first from left to right.

## Apple /// Hires

This is the third new graphics mode. It has 140 by 192 pixel resolution, and 1 of 16 color selection per pixel. In this mode the pixel is formed by a group of four dots of the same color.

There are two distinct screen pages in this mode but the mapping of the individual pages is, at first encounter, a bit difficult to master. Good luck!

- The display dot represents a sequence of 4 data bits in the ram display area.
- Two rams are used starting at 2000 and 4000 respectively and alternate bytes are fetched from each ram area.
- In any video mode only 7 of the 8 bits of each byte are displayed.

With this information in mind...and remembering that each pixel in this mode is made from 4 bits...you can see that you need 4 bytes of information to get 7 pixels. The way in which these bytes map into picture elements is shown below.

It is apparent, from the diagram, that picture elements overlap the byte boundaries for 7 picture elements and 4 bytes. The basic pattern then repeats.

The four bytes are shifted out in a fashion similar to the other Apple /// modes:

- The first byte comes from the primary and the second byte comes from the secondary.
- The first byte contains the first pixel and the second byte comes from the secondary.
- The first byte contains the first pixel and 3 bits of the second pixel.
- The second byte contains the fourth bit of the second pixel, the third pixel, and the first two bits of the fourth pixel.
- The third byte contains the last two bits of the fourth pixel, the fifth pixel, and the first bit of the sixth pixel.
- The fourth byte contains the last three bits of the sixth pixel and the entire seventh pixel.

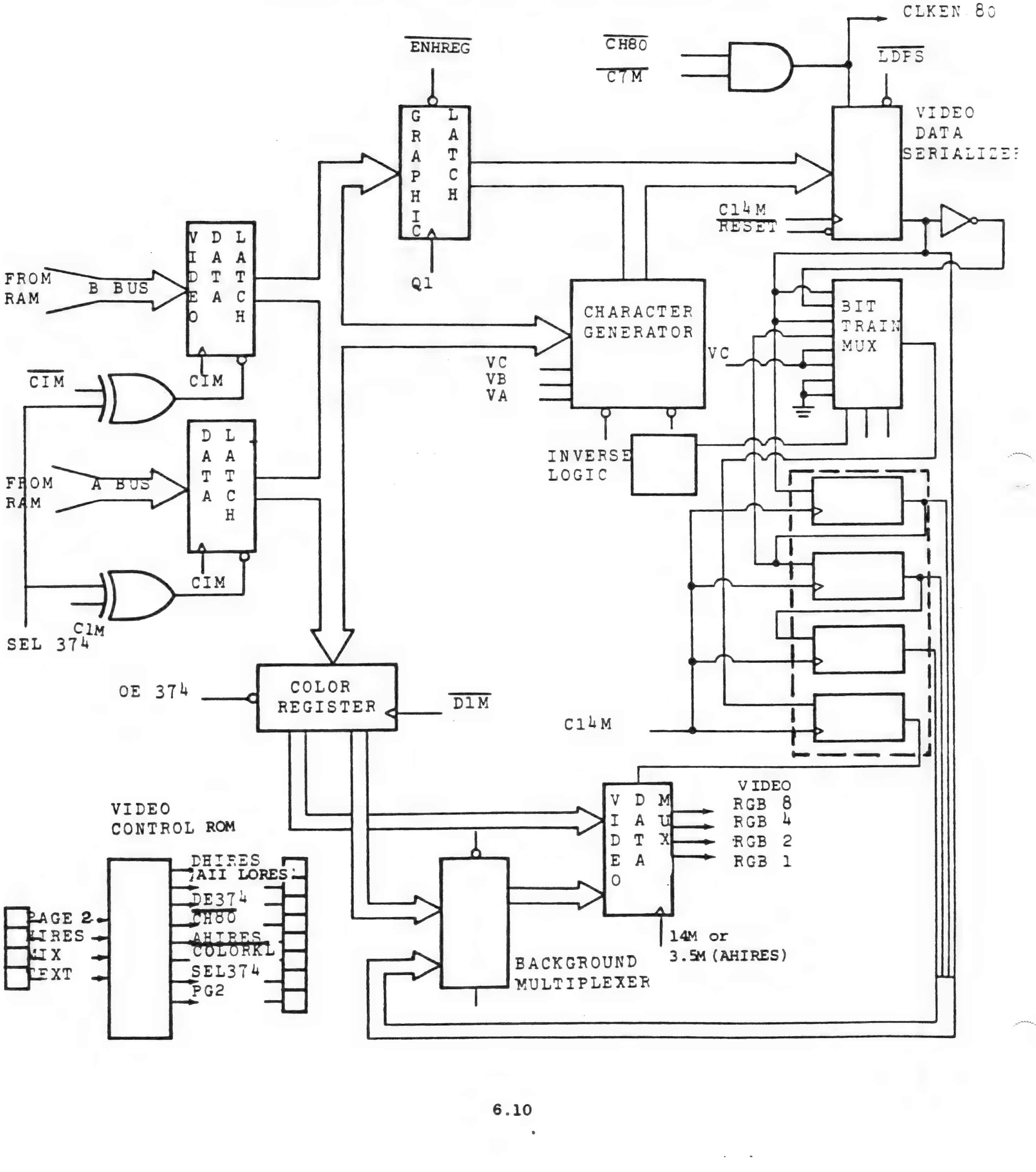
We hope the preceding diagram will help you picture what has already been described.

For this mode, Page 1 is mapped with the primary fetch in 2000-3FFF, and the secondary in 4000-5FFF. In Page 2 the primary is in 6000-7FFF, and the secondary is in 8000-7FFF.

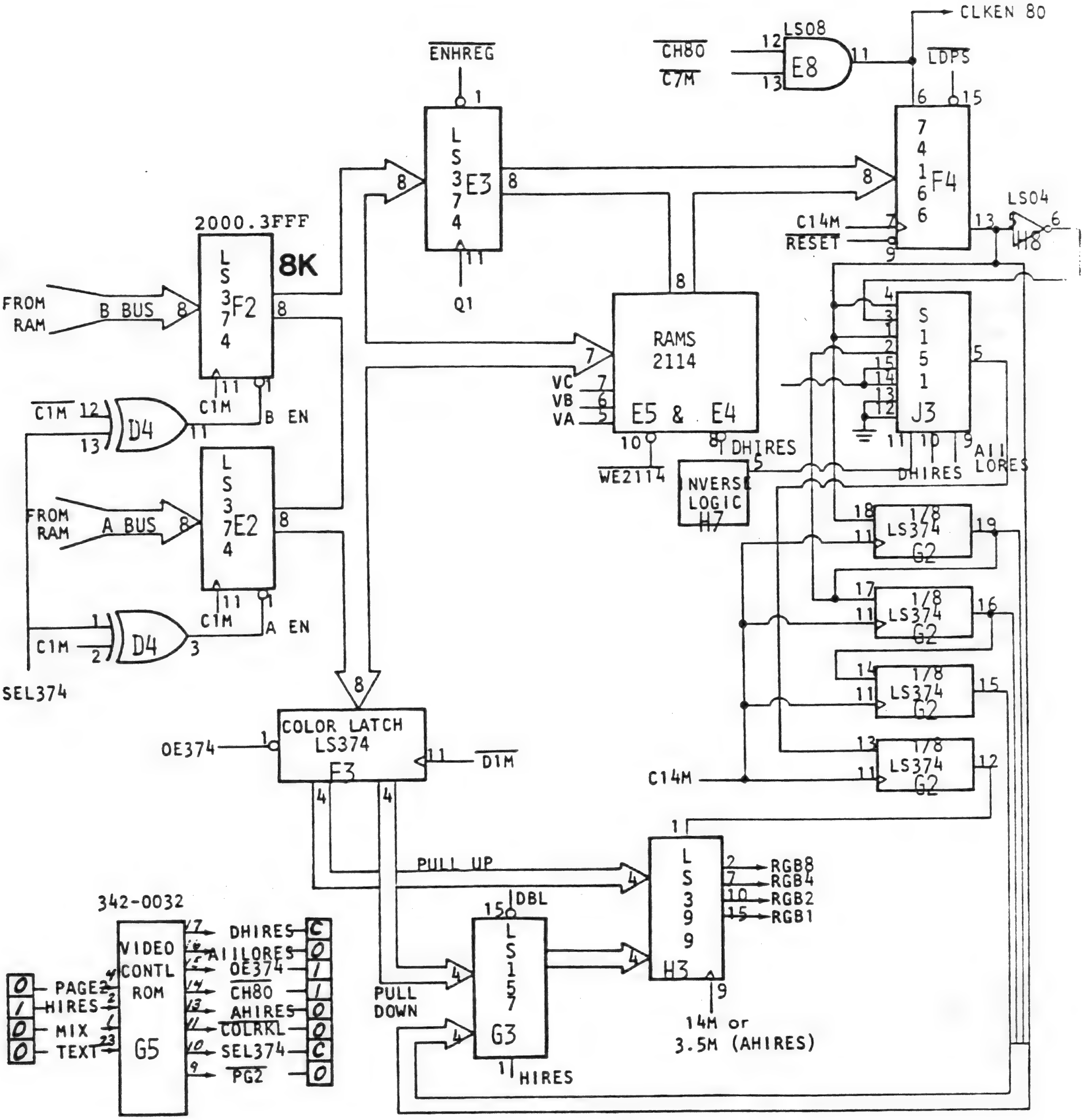
# APPENDIX (VIDEO)

- Apple /// Video Logic Block Diagram
- Video Logic Diagrams for:
  1. Hires Mode Page 1, B/W 280 X 192
  2. Hires Mode Page 2, B/W 280 X 192
  3. Color Hires Mode Page 1, 280 X 192
  4. Color Hires Mode Page 2, 280 X 192
  5. Super Hires Mode Page 1, 560 X 192
  6. Super Hires Mode Page 2, 560 X 192
  7. Ahires Test Page 1, 140 X 192
  8. Ahires Test Page 2, 140 X 192
  9. Color Bar & Grey Scale Test
  10. Apple II Text Mode Page 1, B & W, 40 Column
  11. Apple II Test Mode Page 2, B & W, 40 Column
  12. Sara 40 Column Text Mode Test, 16 Colors
  13. Sara 80 Column Text Mode Test, B & W
- Apple /// Video Modes Truth Tables
- Video Prom Listing
- Video Prom Equivalent Logic

# APPLE III VIDEO LOGIC BLOCK DIAGRAM

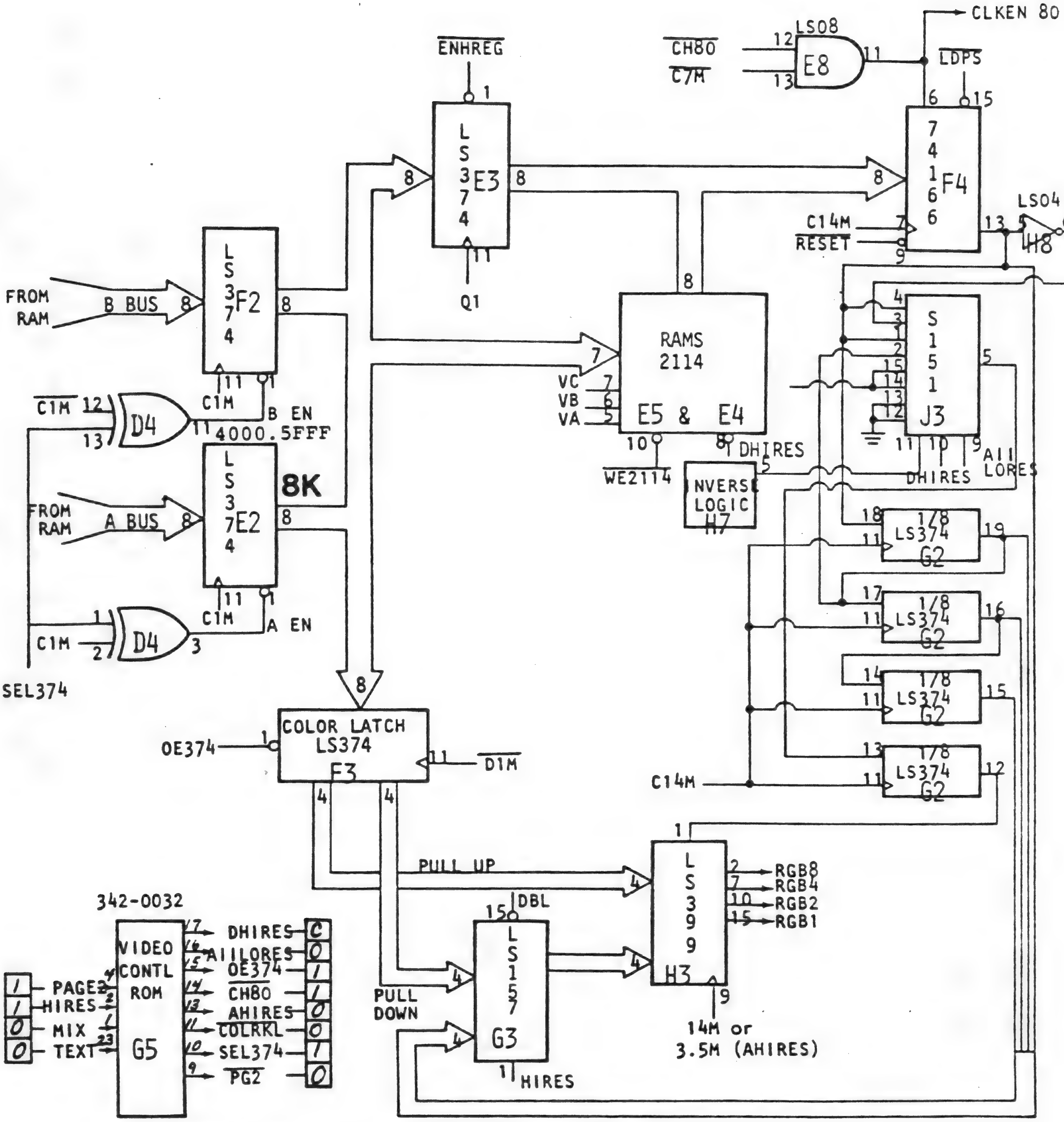

CLKEN 80
ENHREG
CH80
C7M
LDPS
GRAPHIC LATCH
VIDEO DATA SERIALIZE
C14M
RESET
Q1
FROM RAM
B BUS
VIDEO DATA LATCH
CHARACTER GENERATOR
VC
VB
VA
VC
BIT TRAIN MUX
CIM
CIM
INVERSE LOGIC
FROM RAM
A BUS
DATA LATCH
CIM
C1M
SEL 374
OE 374
COLOR REGISTER
D1M
C14M
VIDEO CONTROL ROM
DHIRES
AII LORES
DE374
CH80
AHIRES
COLORKL
SEL374
PG2
PAGE 2
HIRES
MIX
TEXT
BACKGROUND MULTIPLEXER
VIDEO DATA MUX
VIDEO
RGB 8
RGB 4
RGB 2
RGB 1
14M or 3.5M (AHIRES)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
LS374 E3
74166 F4
LS04
H8
C14M
RESET
Q1
2000.3FFF
8K
LS374 F2
FROM RAM
B BUS
C1M
B EN
D4
RAMS 2114
E5 & E4
VC
VB
VA
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
AII LORES
LS374 E2
A BUS
A EN
SEL374
1/8 LS374 G2
COLOR LATCH LS374 F3
OE374
D1M
C14M
PULL UP
PULL DOWN
LS399 H3
RGB8
RGB4
RGB2
RGB1
LS157 G3
DBL
HIRES
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2
0
1
0
0
C
0
1
1
0
0
C
0

1. HIRES MODE PAGE 1 - B & W - 280 X 192
2000.3FFF (8K)

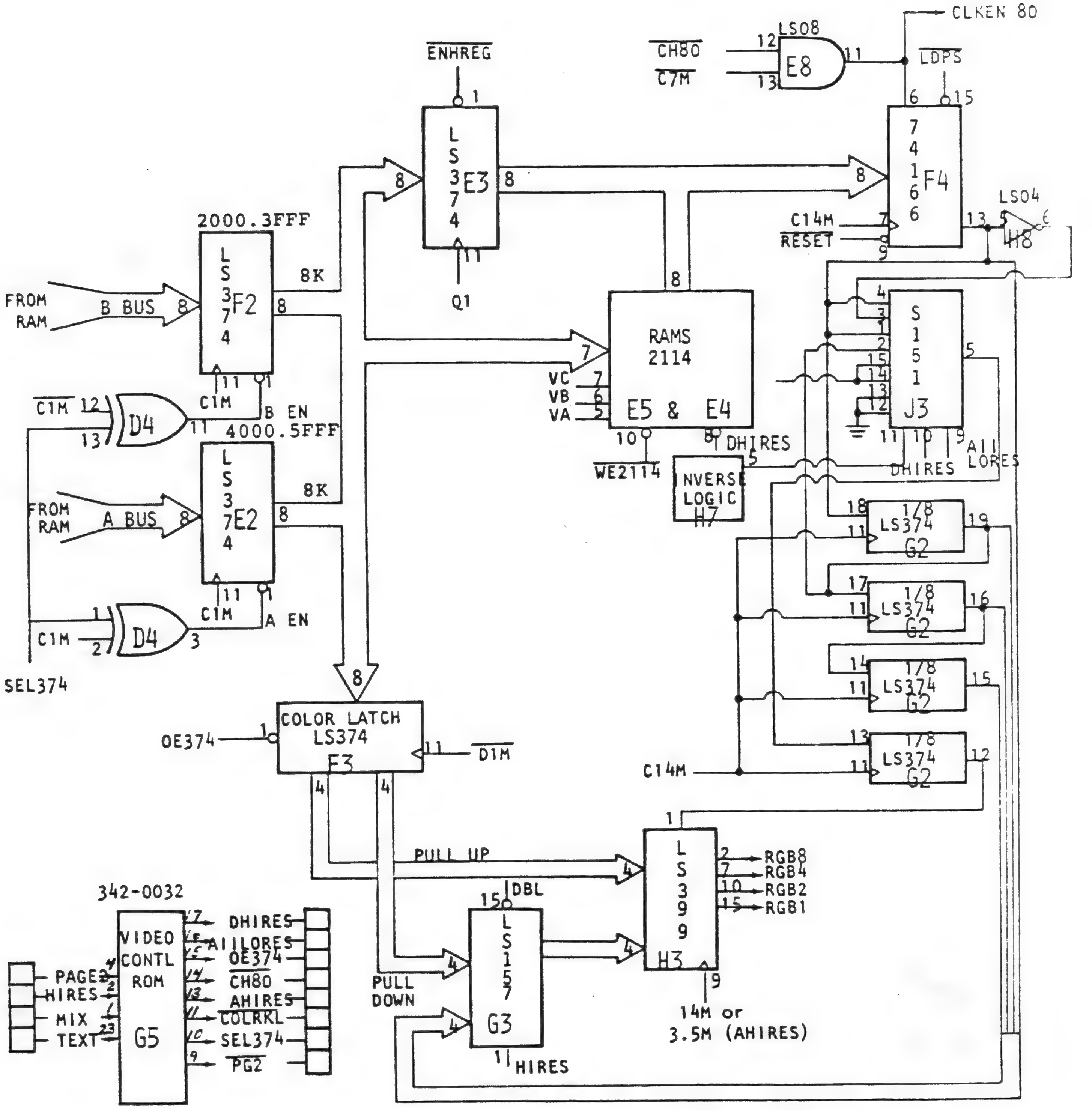
# A/// VIDEO LOGIC DIAGRAM



ENHREG
LS08
CH80
C7M
E8
CLKEN 80
LDPS
LS374 E3
74166 F4
C14M
RESET
LS04
H8
Q1
FROM RAM
B BUS
LS374 F2
C1M
B EN
D4
4000.5FFF
8K
LS374 E2
A BUS
A EN
SEL374
RAMS 2114
VC
VB
VA
E5 & E4
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
ALL LORES
LS374 G2
1/8
C14M
COLOR LATCH LS374 F3
OE374
D1M
PULL UP
PULL DOWN
LS399 H3
RGB8
RGB4
RGB2
RGB1
LS157 G3
DBL
HIRES
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

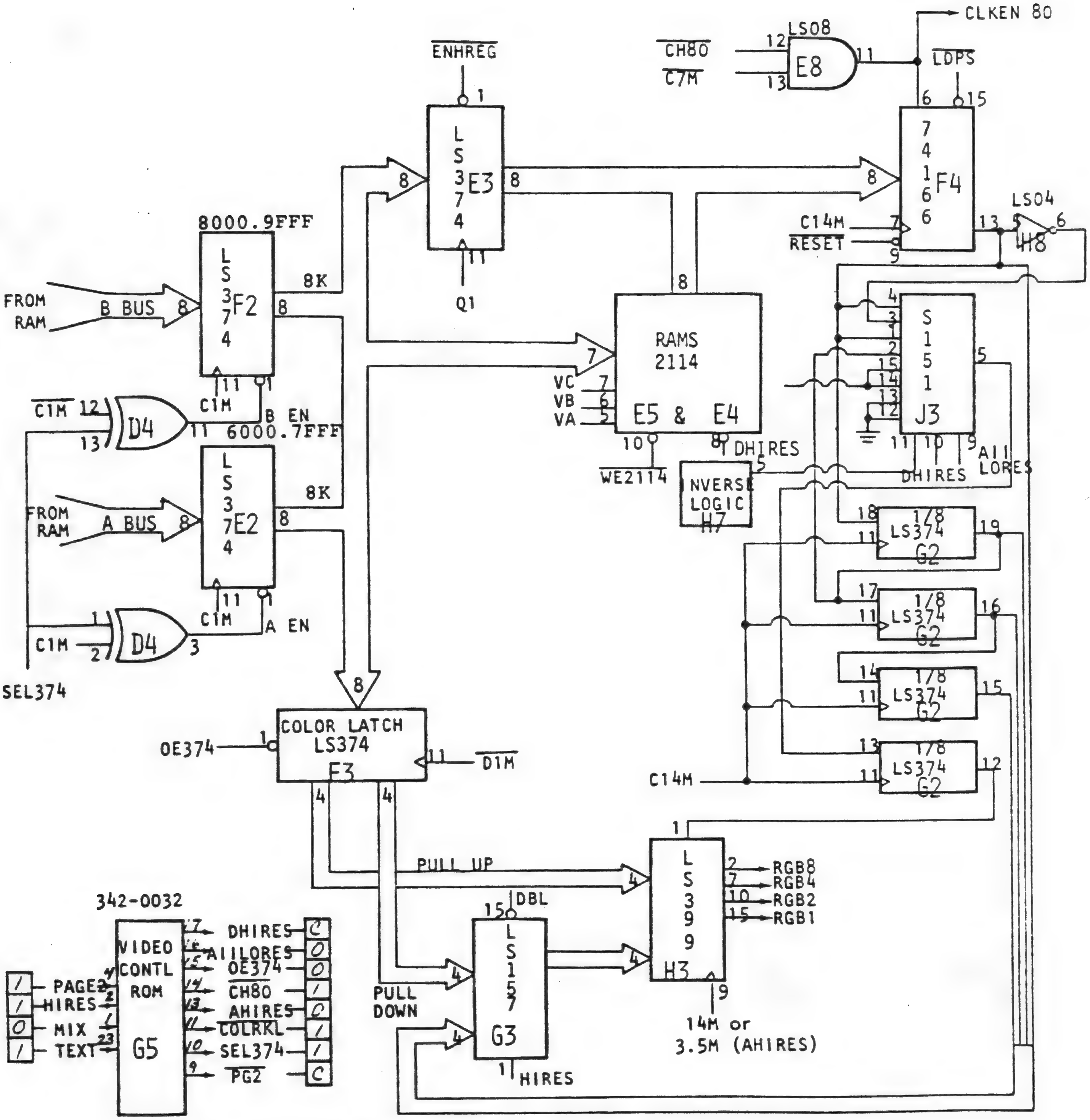
2. HIRES MODE PAGE 2 - B & W - 280 X 192
4000.5FFF (8K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
12
13
E8
11
LDPS
6
15
74166
F4
8
C14M
7
RESET
9
13
LS04
5
6
H8
ENHREG
1
LS374
E3
8
8
11
Q1
2000.3FFF
LS374
F2
FROM RAM
B BUS
8
8
8K
11
1
C1M
B EN
C1M
12
13
D4
11
4000.5FFF
LS374
E2
FROM RAM
A BUS
8
8
8K
11
1
C1M
A EN
C1M
1
2
D4
3
SEL374
8
7
RAMS 2114
VC
VB
VA
7
6
5
E5 & E4
10
8
WE2114
DHIRES
5
INVERSE LOGIC
H7
4
3
1
2
15
14
13
12
S151
J3
5
11
10
9
DHIRES
AIILORES
18
11
1/8 LS374
G2
19
17
11
1/8 LS374
G2
16
14
11
1/8 LS374
G2
15
13
11
1/8 LS374
G2
12
C14M
8
COLOR LATCH LS374
F3
OE374
1
11
D1M
4
4
PULL UP
4
1
LS399
H3
2
7
10
15
RGB8
RGB4
RGB2
RGB1
4
9
14M or 3.5M (AHIRES)
15
DBL
LS157
G3
4
4
1
HIRES
PULL DOWN
342-0032
VIDEO CONTL ROM
G5
PAGE2
HIRES
MIX
TEXT
4
2
1
23
17
16
15
14
13
11
10
9
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

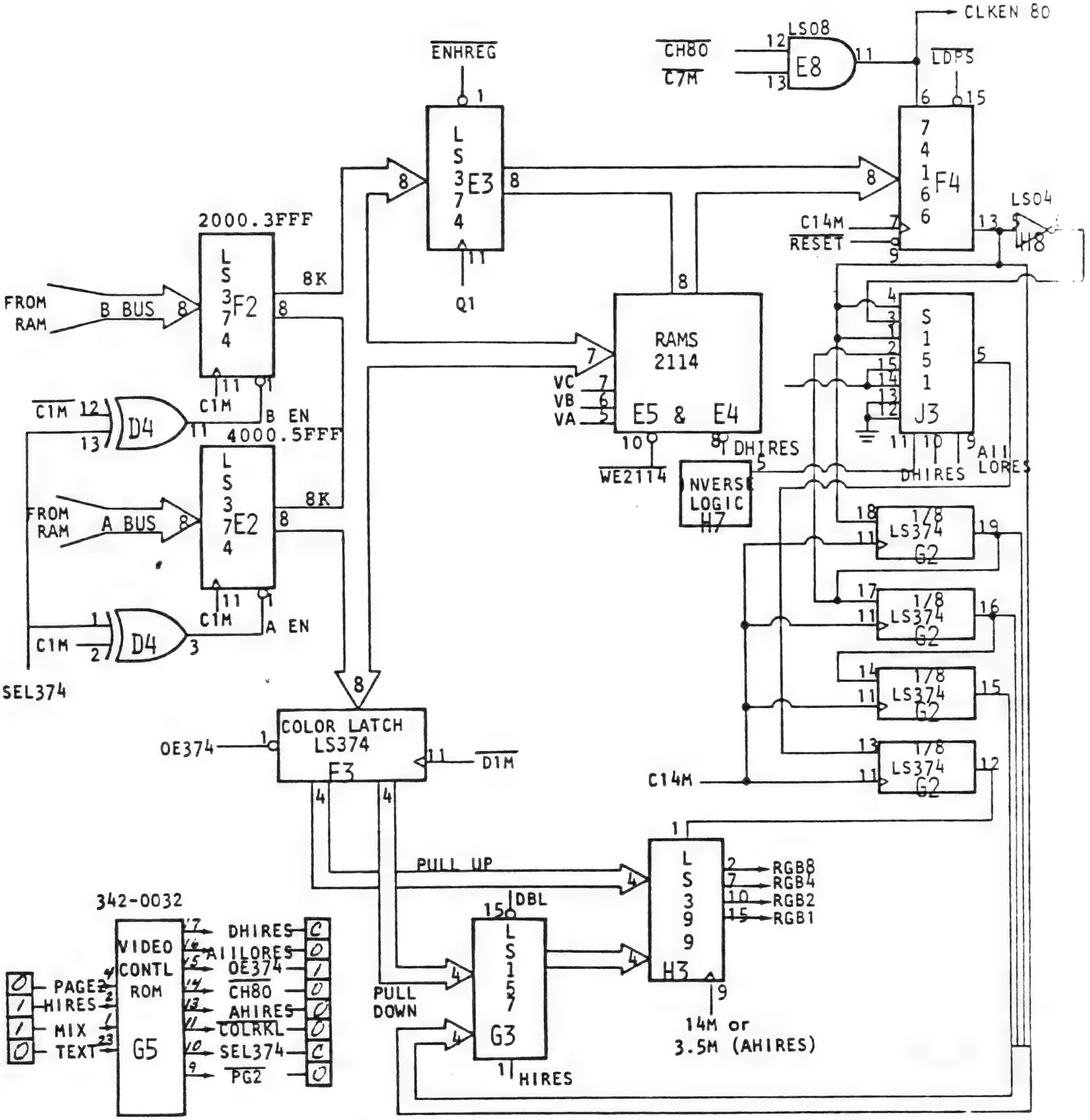
3. 280 X 192 COLOR HIRES MODE PAGE 1 ( FGD/BKGD HIRES)
2000.5FFF (16K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
L S 3 7 4 E3
Q1
7 4 1 6 6 F4
C14M
RESET
LS04
H8
8000.9FFF
FROM RAM
B BUS
L S 3 7 4 F2
8K
C1M
B EN
D4
6000.7FFF
RAMS 2114
VC
VB
VA
E5 & E4
WE2114
DHIRES
INVERSE LOGIC H7
S 1 5 1 J3
DHIRES
AII LORES
FROM RAM
A BUS
L S 3 7 4 E2
A EN
SEL374
1/8 LS374 G2
1/8 LS374 G2
1/8 LS374 G2
1/8 LS374 G2
C14M
COLOR LATCH LS374 F3
OE374
D1M
PULL UP
PULL DOWN
L S 3 9 9 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
DBL
L S 1 5 7 G3
HIRES
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2
1
1
0
1
C
0
0
1
C
1
1
C

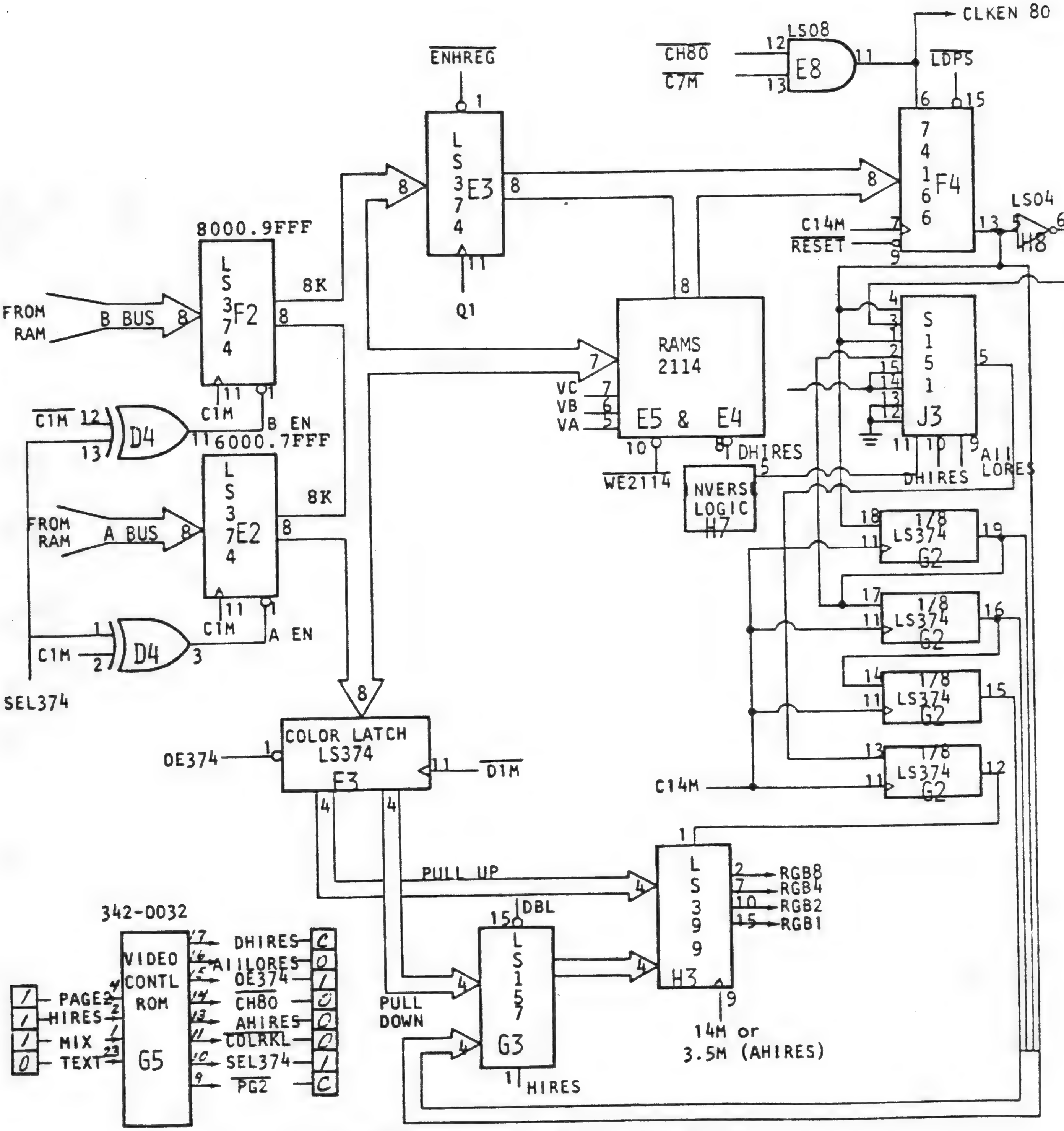
4. 280 X 192 COLOR HIRES MODE PAGE 2 (FGB/BKGD HIRES)
6000.9FFF (16K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
LS374 E3
74166 F4
C14M
RESET
LS04
H8
2000.3FFF
LS374 F2
8K
Q1
FROM RAM
B BUS
C1M
B EN
D4
4000.5FFF
RAMS 2114
VC
VB
VA
E5 & E4
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
A11 LORES
DHIRES
1/8 LS374 G2
FROM RAM
A BUS
LS374 E2
A EN
SEL374
COLOR LATCH LS374 F3
OE374
D1M
C14M
PULL UP
PULL DOWN
DBL
LS157 G3
HIRES
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
A11LORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

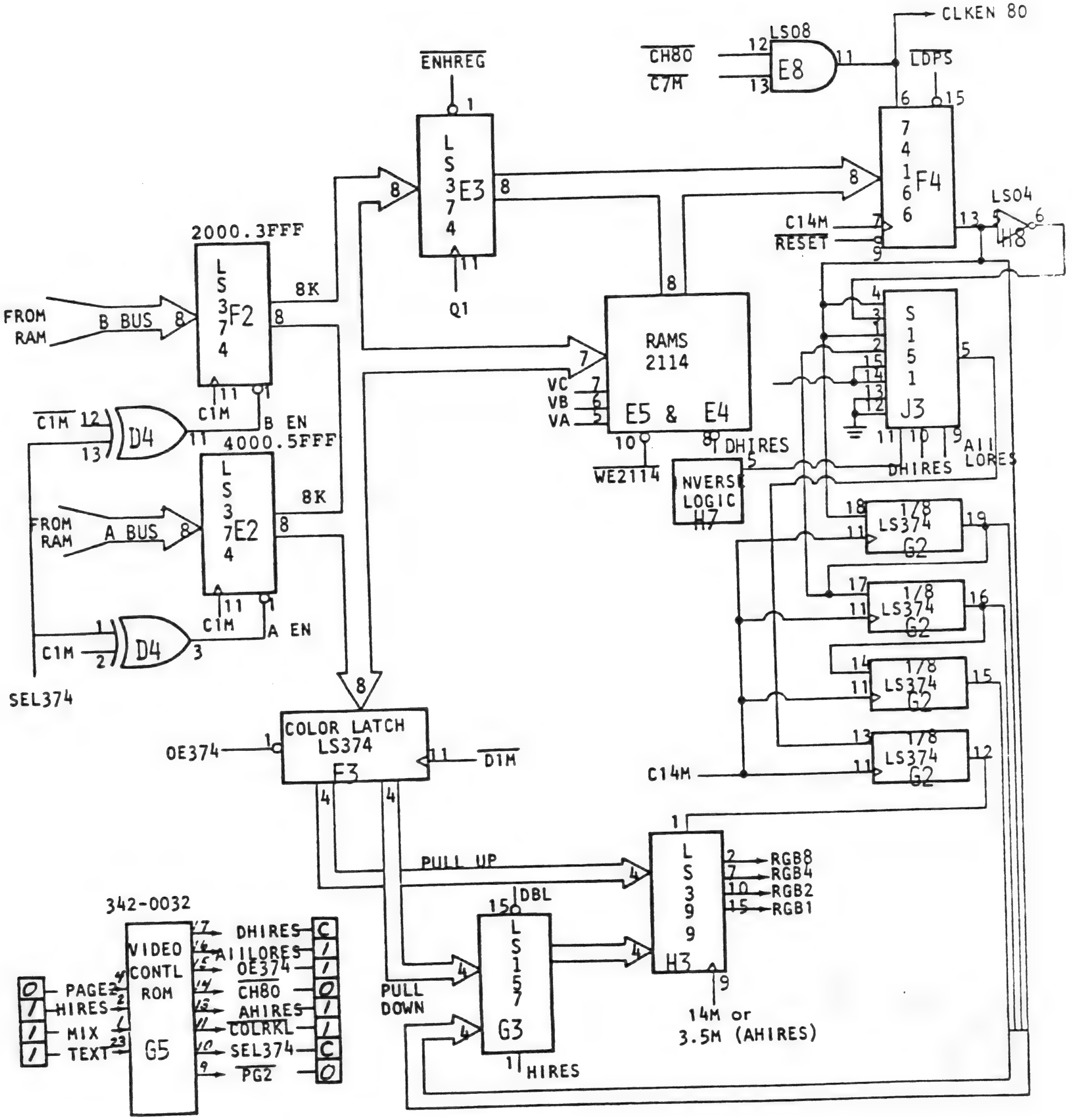
5. SUPER HIRES MODE PAGE 1 - B & W - 560X192
2000.5FFF (16K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
E8
CH80
C7M
LDPS
ENHREG
LS374 E3
Q1
74166 F4
C14M
RESET
LS04
H8
8000.9FFF
LS374 F2
FROM RAM
B BUS
8K
RAMS 2114
E5 & E4
VC
VB
VA
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
DHIRES
AII LORES
C1M
D4
B EN
6000.7FFF
LS374 E2
A BUS
A EN
SEL374
1/8 LS374 G2
C14M
COLOR LATCH LS374 F3
OE374
D1M
PULL UP
PULL DOWN
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
DBL
LS157 G3
HIRES
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2
1
1
1
0
C
0
1
0
0
0
1
C

6. SUPER HIRES MODE PAGE 2 - B & W - 560 X 192
6000.9FFF (16K)

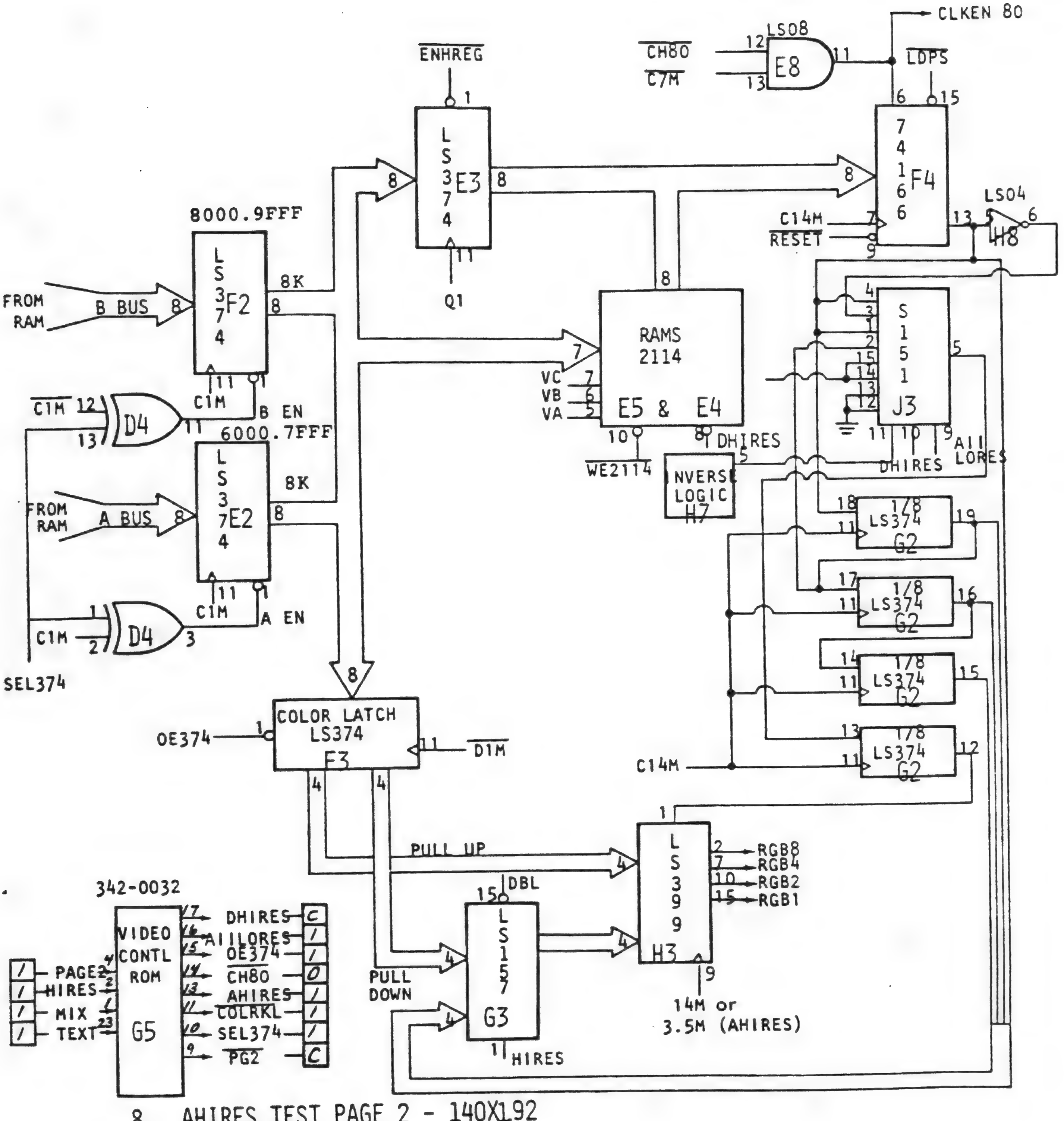
# A/// VIDEO LOGIC DIAGRAM



CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
LS374 E3
7 4 1 6 6 F4
C14M
RESET
LS04
H8
Q1
2000.3FFF
LS374 F2
8K
FROM RAM
B BUS
C1M
B EN
D4
4000.5FFF
RAMS 2114
E5 & E4
VC
VB
VA
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
A11 LORES
LS374 E2
A BUS
A EN
SEL374
1/8 LS374 G2
COLOR LATCH LS374 F3
OE374
D1M
C14M
PULL UP
PULL DOWN
DBL
LS157 G3
HIRES
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
A11LORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

7. AHIRES TEST PAGE 1 - 140X192
2000.5FFF (16K)

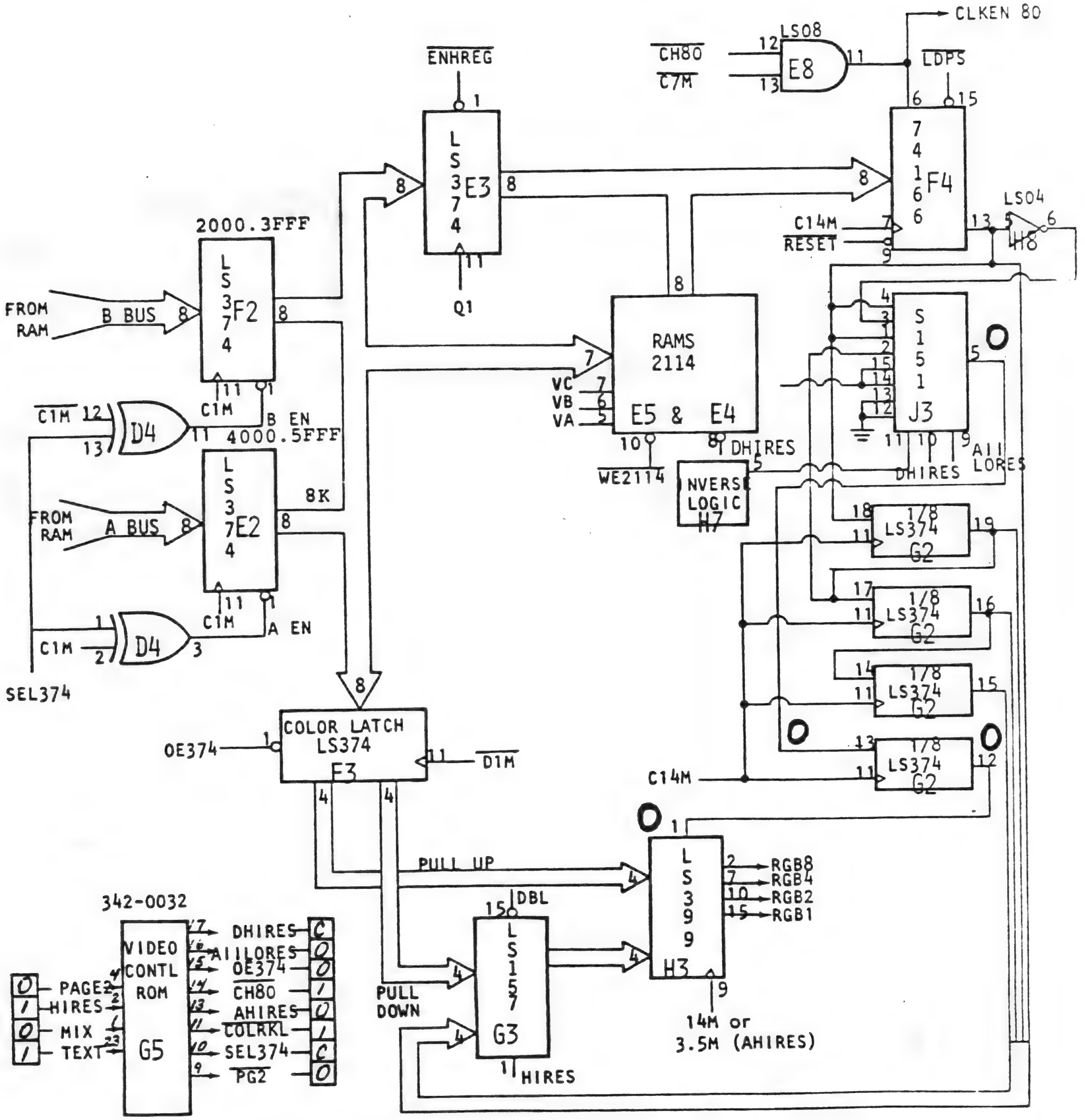
# A/// VIDEO LOGIC DIAGRAM



CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
LS374 E3
74166 F4
LS04
H8
C14M
RESET
Q1
8000.9FFF
LS374 F2
8K
FROM RAM
B BUS
C1M
B EN
D4
6000.7FFF
LS374 E2
A BUS
A EN
SEL374
RAMS 2114
VC
VB
VA
E5 & E4
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
AIILORES
1/8 LS374 G2
COLOR LATCH LS374 F3
OE374
D1M
PULL UP
PULL DOWN
LS157 G3
DBL
HIRES
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
PAGE2
HIRES
MIX
TEXT
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

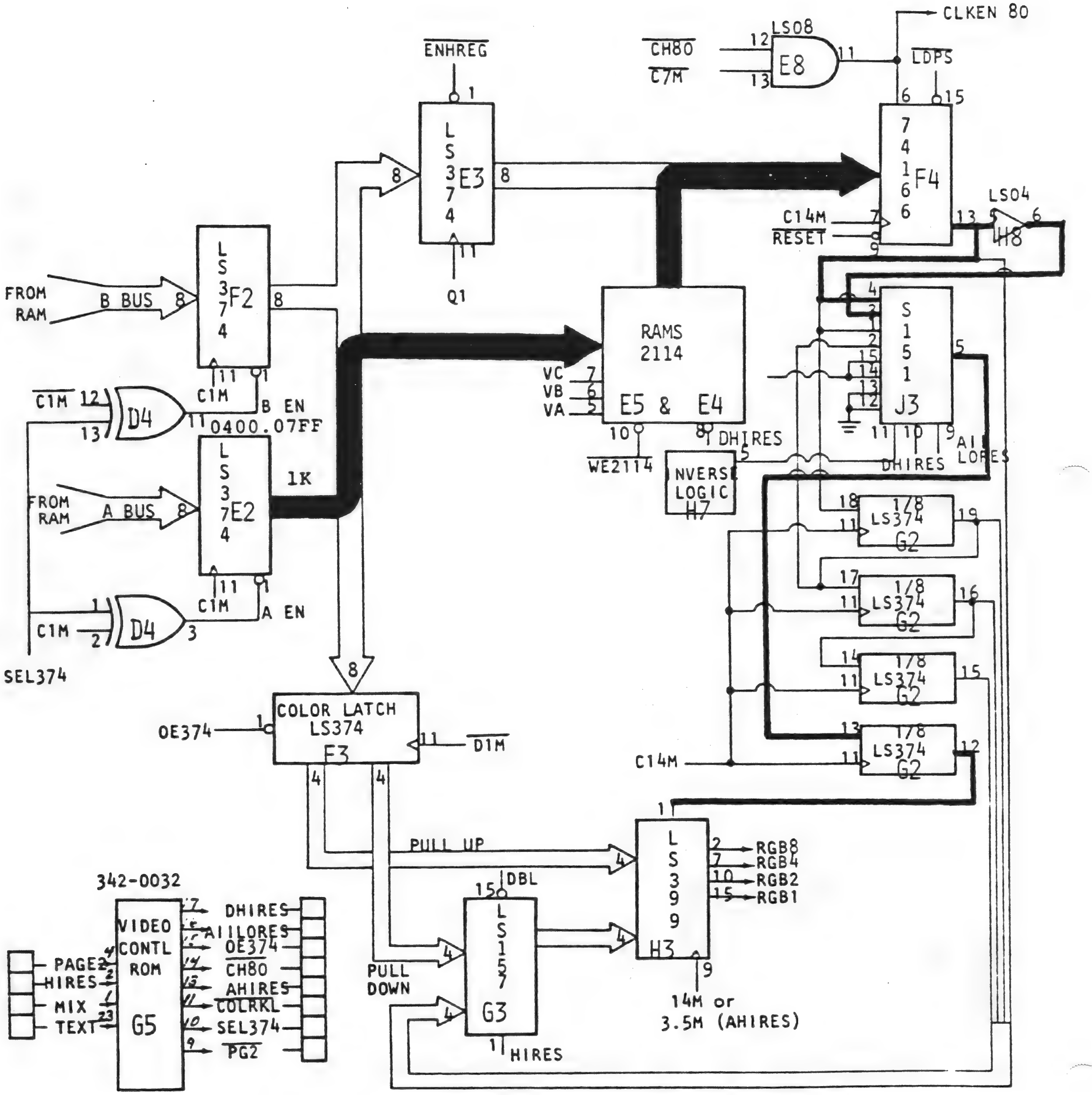
8. AHIRES TEST PAGE 2 - 140X192
6000.9FFF (16K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
12
13
11
E8
CH80
C7M
LDPS
6
15
7
4
1
6
6
F4
8
LS04
5
6
H8
13
C14M
RESET
9
ENHREG
1
L
S
3
7
4
E3
8
11
Q1
2000.3FFF
L
S
3
7
4
F2
FROM RAM
B BUS
8
C1M
B EN
C1M
12
13
D4
11
4000.5FFF
8K
L
S
3
7
4
E2
FROM RAM
A BUS
8
C1M
A EN
1
2
D4
3
SEL374
RAMS
2114
E5 & E4
7
VC
VB
VA
10
WE2114
DHIRES
INVERSE LOGIC
H7
S
1
5
1
J3
4
3
2
15
14
13
12
11
10
9
5
DHIRES
AII LORES
0
1/8
LS374
G2
18
19
17
16
14
15
13
12
11
0
0
C14M
COLOR LATCH
LS374
F3
OE374
D1M
4
4
PULL UP
PULL DOWN
0
L
S
3
9
9
H3
1
RGB8
RGB4
RGB2
RGB1
9
14M or
3.5M (AHIRES)
L
S
1
5
7
G3
DBL
15
HIRES
1
342-0032
VIDEO
CONTL
ROM
G5
0 PAGE2
1 HIRES
0 MIX
1 TEXT
4
2
6
23
17 DHIRES C
16 AIILORES 0
15 OE374 0
14 CH80 1
13 AHIRES 0
11 COLRKL 1
10 SEL374 C
9 PG2 0

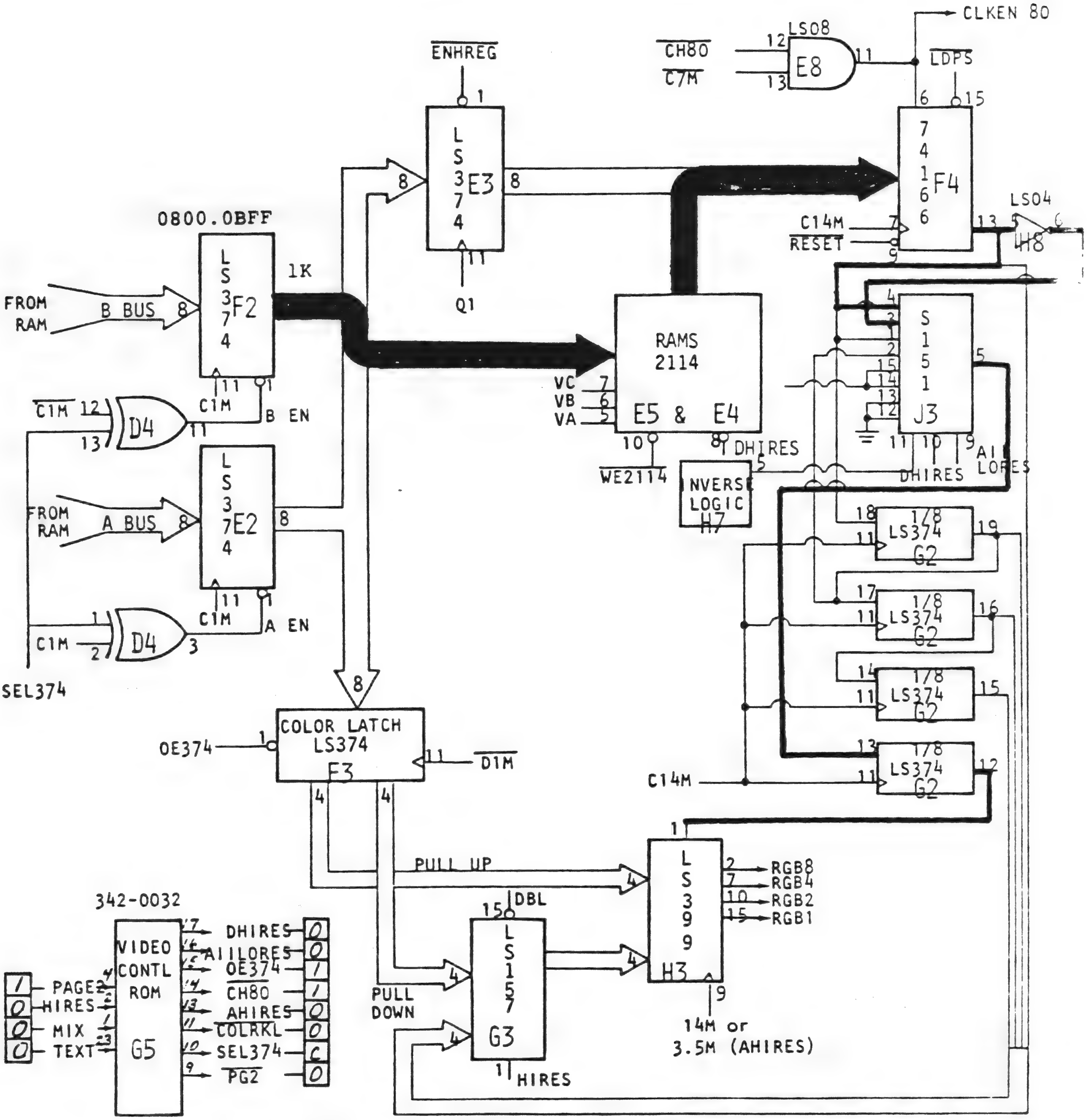
9. COLOR BAR & GRAY SCALE TEST
2000.5FFF (16K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
12
13
E8
11
LDPS
6
15
ENHREG
1
L S 3 7 4
E3
8
8
11
Q1
7 4 1 6 6
F4
C14M
RESET
7
9
13
LS04
5
6
H8
FROM RAM
B BUS
8
L S 3 7 4
F2
8
11
1
C1M
B EN
C1M
12
13
D4
11
0400.07FF
RAMS 2114
VC
VB
VA
7
6
5
E5 & E4
10
8
WE2114
DHIRES
5
INVERSE LOGIC
H7
S 1 5 1
J3
4
3
1
2
15
14
13
12
5
11
10
9
DHIRES
AIILORES
L S 3 7 4
E2
1K
FROM RAM
A BUS
8
11
1
C1M
A EN
C1M
1
2
D4
3
SEL374
18
1/8 LS374
G2
11
19
17
1/8 LS374
G2
11
16
14
1/8 LS374
G2
11
15
13
1/8 LS374
G2
11
12
C14M
8
COLOR LATCH LS374
F3
OE374
1
11
D1M
4
4
PULL UP
4
1
L S 3 9 9
H3
2
RGB8
7
RGB4
10
RGB2
15
RGB1
4
9
14M or 3.5M (AHIRES)
15
DBL
L S 1 5 7
G3
4
4
PULL DOWN
1
HIRES
342-0032
VIDEO CONTL ROM
G5
PAGE2
HIRES
MIX
TEXT
4
3
1
23
17
16
15
14
13
11
10
9
DHIRES
AIILORES
OE374
CH80
AHIRES
COLRKL
SEL374
PG2

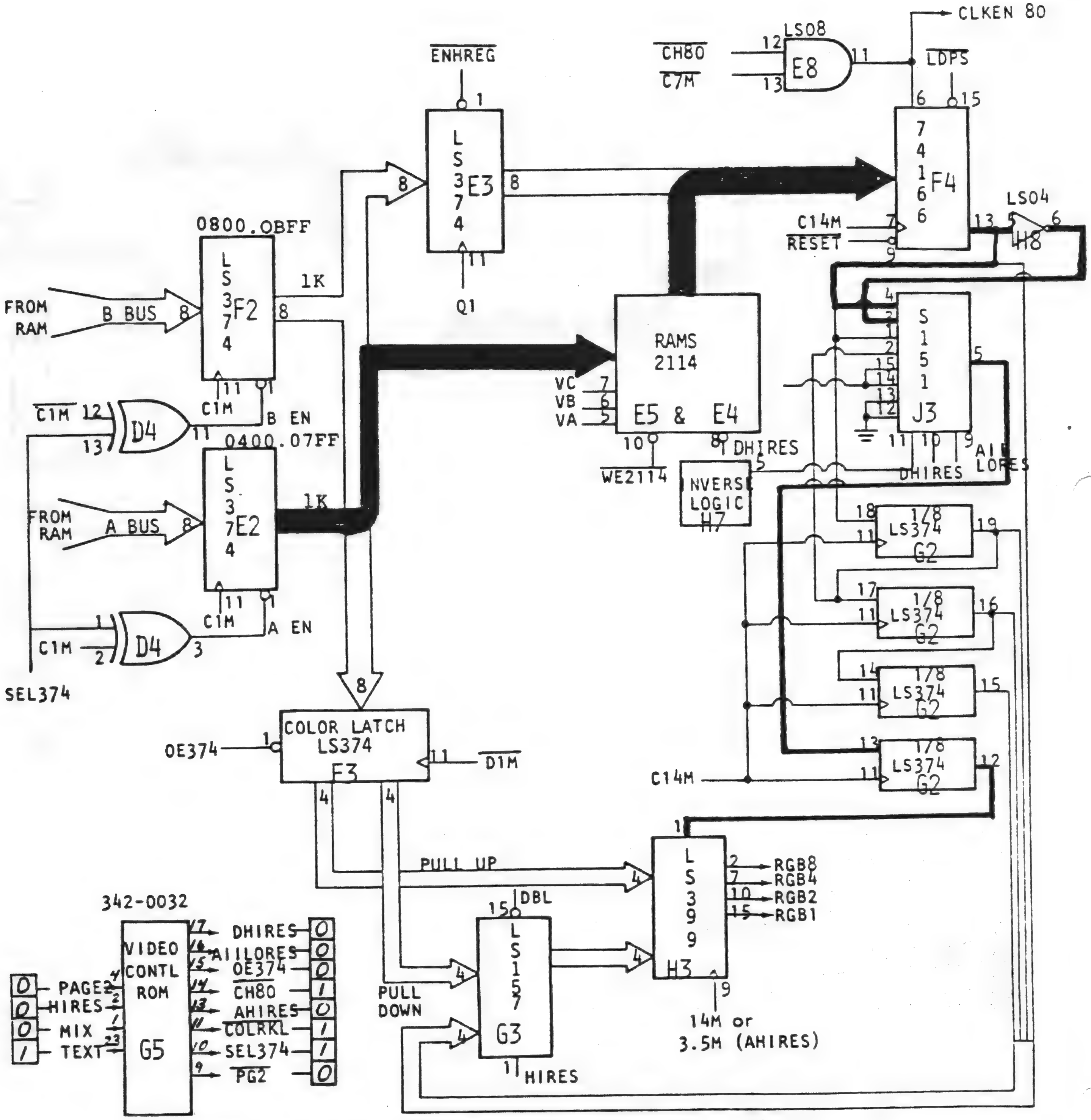
10. APPLE II TEXT MODE PAGE 1 - B & W - 40 COLUMN
0400.07FF (1K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
E8
LDPS
74166 F4
ENHREG
LS374 E3
8
Q1
0800.0BFF
LS374 F2
1K
FROM RAM
B BUS
C1M
B EN
D4
C1M
SEL374
LS374 E2
FROM RAM
A BUS
A EN
RAMS 2114
E5 & E4
VC
VB
VA
WE2114
DHIRES
INVERSE LOGIC H7
C14M
RESET
LS04
H8
S151 J3
DHIRES
AII LORES
1/8 LS374 G2
C14M
COLOR LATCH LS374 F3
OE374
D1M
PULL UP
PULL DOWN
LS157 G3
DBL
HIRES
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
1 PAGE2
0 HIRES
0 MIX
0 TEXT
DHIRES 0
AIILORES 0
OE374 1
CH80 1
AHIRES 0
COLRKL 0
SEL374 C
PG2 0

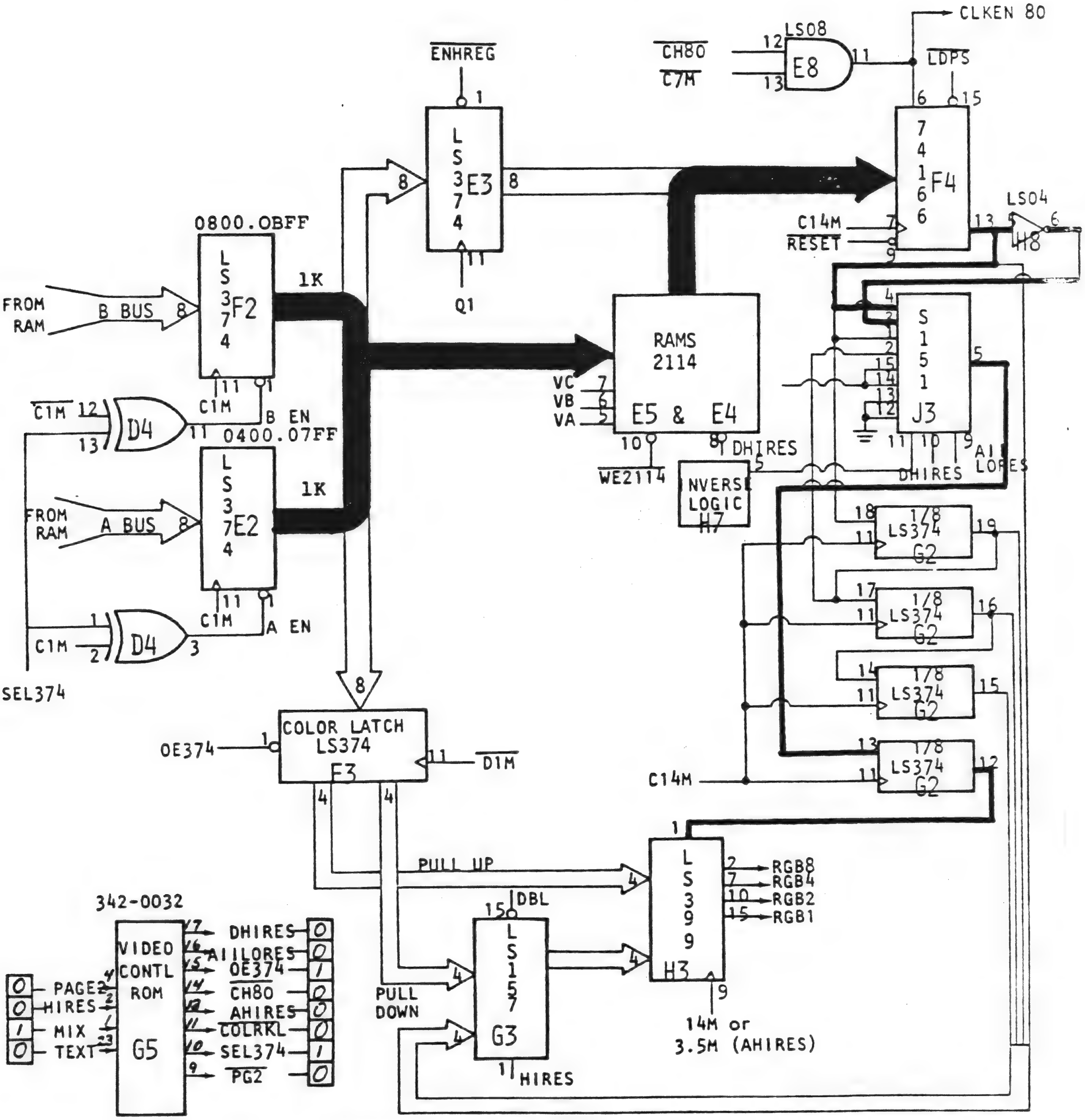
11. APPLE II TEST MODE PAGE 2 - B & W - 40 COLUMN
0800-0BFF (1K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
E8
LDPS
ENHREG
LS374 E3
Q1
74166 F4
C14M
RESET
LS04
H8
0800.0BFF
LS374 F2
1K
FROM RAM
B BUS
C1M
D4
B EN
0400.07FF
RAMS 2114
VC
VB
VA
E5 & E4
WE2114
DHIRES
INVERSE LOGIC H7
S151 J3
AII LORES
FROM RAM
A BUS
LS374 E2
A EN
SEL374
COLOR LATCH LS374 F3
OE374
D1M
1/8 LS374 G2
C14M
PULL UP
PULL DOWN
DBL
LS157 G3
HIRES
LS399 H3
RGB8
RGB4
RGB2
RGB1
14M or 3.5M (AHIRES)
342-0032
VIDEO CONTL ROM G5
0 PAGE2
0 HIRES
0 MIX
1 TEXT
DHIRES 0
AIILORES 0
OE374 0
CH80 1
AHIRES 0
COLRKL 1
SEL374 1
PG2 0

12. SARA 40 COLUMN TEXT MODE TEST- 16 COLORS
0400.0BFF (2K)

# A/// VIDEO LOGIC DIAGRAM


CLKEN 80
LS08
CH80
C7M
12
13
E8
11
LDPS
6
15
74166
F4
ENHREG
1
LS374
E3
8
8
11
Q1
C14M
RESET
7
9
13
LS04
5
H8
6
0800.0BFF
LS374
F2
1K
FROM RAM
B BUS
8
11
1
C1M
B EN
C1M
12
13
D4
11
0400.07FF
RAMS 2114
E5 & E4
VC
VB
VA
7
6
5
10
8
WE2114
DHIRES
5
INVERSE LOGIC
H7
S151
J3
4
3
2
1
15
14
13
12
11
10
9
5
DHIRES
AII LORES
LS374
E2
1K
FROM RAM
A BUS
8
11
1
C1M
A EN
1
2
C1M
D4
3
SEL374
18
11
1/8 LS374
G2
19
17
11
1/8 LS374
G2
16
14
11
1/8 LS374
G2
15
13
11
1/8 LS374
G2
12
C14M
8
COLOR LATCH
LS374
F3
OE374
1
11
D1M
4
4
PULL UP
PULL DOWN
1
LS399
H3
2
7
10
15
RGB8
RGB4
RGB2
RGB1
9
14M or 3.5M (AHIRES)
DBL
15
LS157
G3
4
4
4
4
1
HIRES
342-0032
VIDEO CONTL ROM
G5
0
PAGE2
4
0
HIRES
2
1
MIX
1
0
TEXT
23
17
DHIRES
0
16
AIILORES
0
15
OE374
1
14
CH80
0
13
AHIRES
0
11
COLRKL
0
10
SEL374
1
9
PG2
0

13. SARA 80 COLUMN TEXT MODE TEST - B & W
0400.0BFF (2K)

# VIDEO MODES

APPLE III

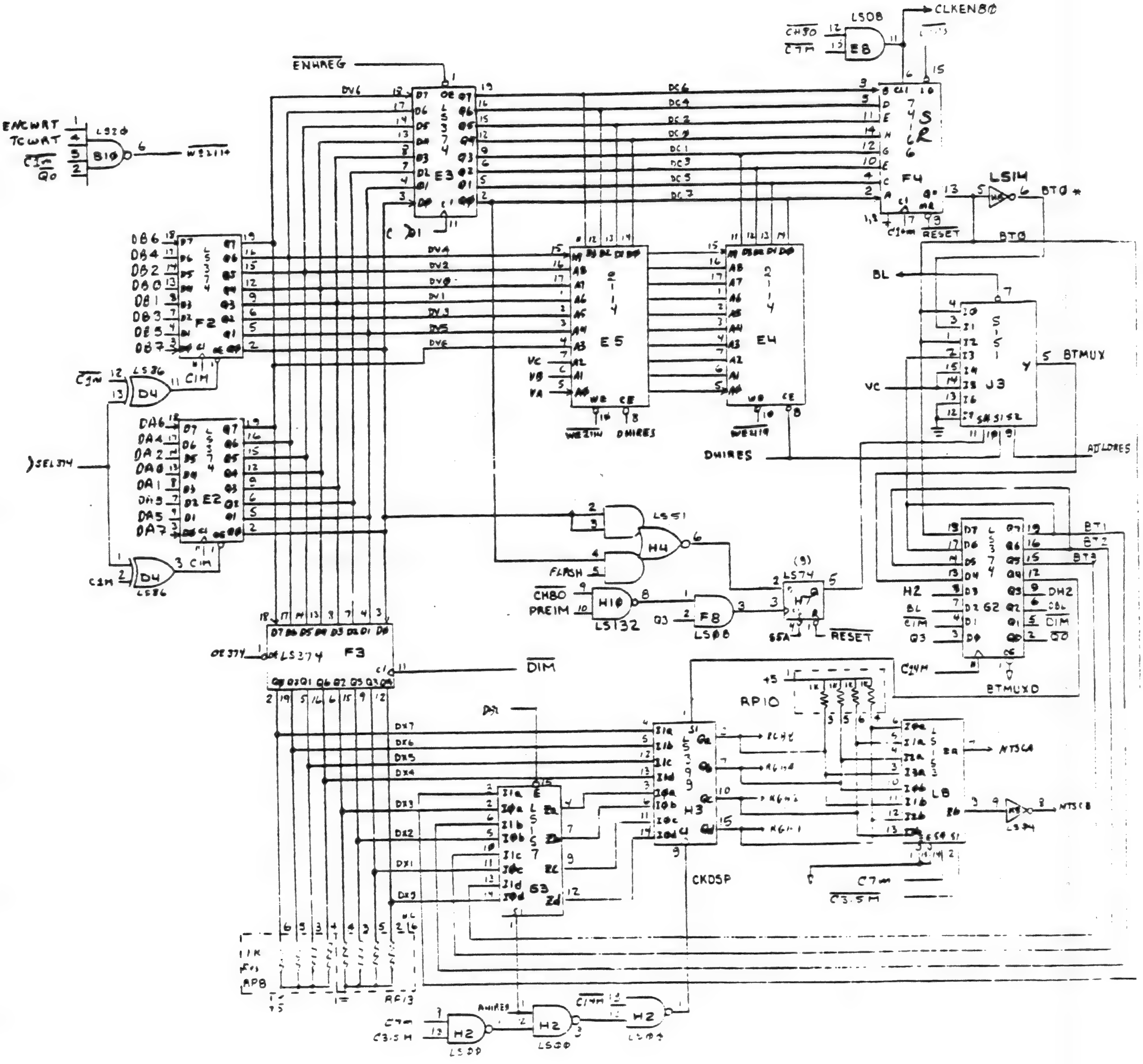
OUTPUTS

INPUTS TO ROM G5 (0032)

OUTPUTS FROM ROM G5 (0032)

| | H6 (9334) pin 7 | H6 (9334) pin 5 | H6 (9334) pin 4 | .6 (9334) pin 6 | PG 2 | SEL 374 | COLOR KL | A HIRES | CH 80 | OE 374 | AII LORES | D HIRES | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ROM G5 pin 2 | ROM G5 pin 1 | ROM G5 pin 23 | ROM G5 pin 4 | G5 pin 9 | G5 pin 10 | G5 pin 11 | G5 pin 13 | G5 pin 14 | G5 pin 15 | G5 pin 16 | G5 pin 17 | |
| | 0 1<br>C056/C057 | 0 1<br>C052/C053 | 0 1<br>C050/C051 | 0 1<br>C054/C055 | | | | | | | | | |
| **PAGE 1** | HIRES | MIX | GR/TEXT | GP1~2 | | | | | | | | | |
| 40 CHAR AII (B/W) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 40 CHARSARA (color) | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 2 |
| 80 CHAR (B/W) | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 3 |
| 80 CHAR (B/W) | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| AII HIRES (280x192, B/W) | 1 | 0 | 0 | 0 | 0 | clocking | 0 | 0 | 1 | 1 | 0 | clocking | 5 |
| FGD/BKGD HIRES (280x192, 16 colors) | 1 | 0 | 1 | 0 | 0 | clocking | 1 | 0 | 1 | 0 | 0 | clocking | 6 |
| SUPER HIRES (560x192, B/W) | 1 | 1 | 0 | 0 | 0 | clocking | 0 | 0 | 0 | 1 | 0 | clocking | 7 |
| 140 x192 AHIRES (140x192, color) | 1 | 1 | 1 | 0 | 0 | clocking | 1 | 1 | 0 | 1 | 1 | clocking | 8 |
| **PAGE 2** | | | | | | | | | | | | | |
| 40 CHAR AII (B/W) | 0 | 0 | 0 | 1 | 0 | clocking | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 40 CHAR SARA (color) | 0 | 0 | 1 | 1 | 0 | clocking | 1 | 0 | 1 | 0 | 0 | 0 | 2 |
| 80 CHAR (B/W) | 0 | 1 | 0 | 1 | 0 | clocking | 0 | 0 | 0 | 1 | 0 | 0 | 3 |
| 80 CHAR (B/W) | 0 | 1 | 1 | 1 | 0 | clocking | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| AII HIRES (280x192, B/W) | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | clocking | 5 |
| FGD/BKGD HIRES (280x192 16 colors) | 1 | 0 | 1 | 1 | clocking | 1 | 1 | 0 | 1 | 0 | 0 | clocking | 6 |
| SUPER HIRES (560x192, B/W) | 1 | 1 | 0 | 1 | clocking | 1 | 0 | 0 | 0 | 1 | 0 | clocking | 7 |
| 140 x 192 AHIRES (140x192 color) | 1 | 1 | 1 | 1 | clocking | 1 | 1 | 1 | 0 | 1 | 1 | clocking | 8 |

≃ 175 nsec ~ 5.7 MHz

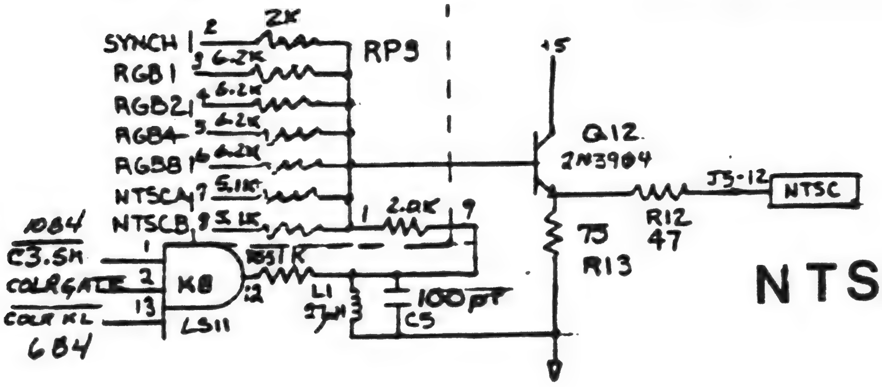

CLKEN80
LS08
E8
CH80
C7M
ENHREG
E3
LS374
F4
74LS166
LS14
BT0
ENCWRT
TCWRT
C1M
Q0
LS20
B10
WE2114
DV6
DC6
DC4
DC2
DC0
DC1
DC3
DC5
DC7
RESET
DB6
DB4
DB2
DB0
DB1
DB3
DB5
DB7
F2
DV4
DV2
DV0
DV1
DV3
DV5
DV7
E5
E4
2114
VC
VB
VA
WE
CE
DHIRES
WE2114
BL
S151
J3
BTMUX
AT LORES
C1M
LS86
D4
DA6
DA4
DA2
DA0
DA1
DA3
DA5
DA7
E2
SEL374
LS51
H4
FLASH
CH80
PREIM
H10
LS132
F8
LS08
LS74
H7
SEA
BT1
BT2
BT3
H2
G2
DH2
CBL
DIM
CD
C14M
BTMUXD
F3
LS274
OE374
DIM
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
+5
RP10
RGB
NTSCA
NTSCB
LS157
G3
LS399
H3
L8
CKDSP
C7M
C3.5M
11K
RP8
RP13
AHIRES
LS00
C14M
H2

## VIDEO OUTPUTS

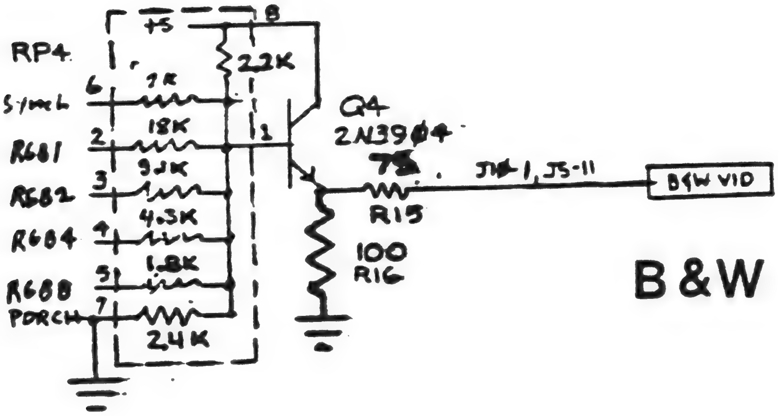
- NTSC COLOR COMPOSITE VIDEO
- NTSC B/W COMPOSITE VIDEO
- SYNC
- FOUR PRIMARY INDEPENDENT VIDEO LINES

- MIX TO FORM RGB APPLE COLORS
  THREE LINES CAN DRIVE TTL RGB MONITOR

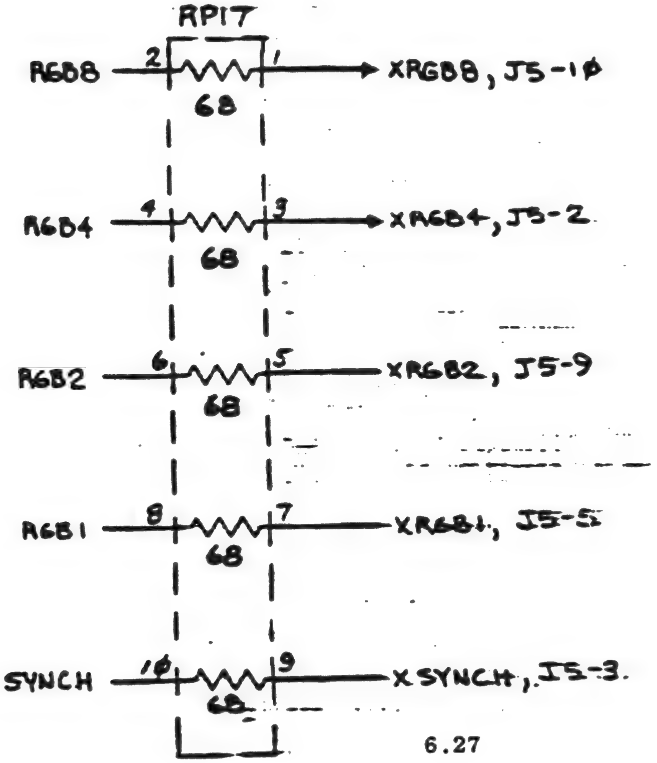
# VIDEO OUTPUTS


SYNCH
RGB1
RGB2
RGB4
RGB8
NTSCA
NTSCB
2K
6.2K
6.2K
6.2K
6.2K
5.1K
5.1K
RP3
2.0K
1
9
10B4
C3.5M
COLRGATE
COLR KL
6B4
K8
LS11
1
2
13
12
1K
L1
27μH
100pF
C5
+5
Q12
2N3904
R12
47
J5-12
NTSC
75
R13

## NTSC


RP4
+5
8
2.2K
6
Synch
1K
2
RGB1
18K
3
RGB2
9.1K
4
RGB4
4.3K
5
RGB8
1.8K
7
PORCH
2.4K
1
Q4
2N3904
75
R15
J14-1, J5-11
B&W VID
100
R16

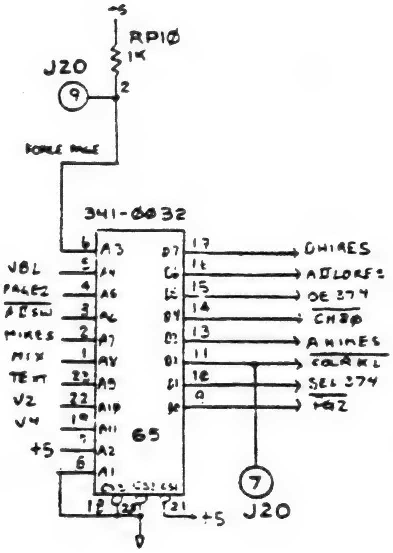
## B&W VIDEO


RP17
RGB8
2
1
68
XRGB8, J5-10
RGB4
4
3
68
XRGB4, J5-2
RGB2
6
5
68
XRGB2, J5-9
RGB1
8
7
68
XRGB1, J5-5
SYNCH
10
9
68
XSYNCH, J5-3

## RGB

ROM 341-0032

A=A
B=B
C=S4
D=VBL
E=PAGE2
F=AIISW'
G=HIRES
H=MIX
I=TEXT
J=V2
K=V4
D0=PG2
D1=SEL374
D2=COLRKL'
D3=AHIRES
D4=CH80'
D5=OE374
D6=AIILORES
D7=DHIRES


+5
RP10
1K
2
J20
9
FORCE PAGE
341-0032
6
A3
VBL
5
A4
PAGE2
4
A5
AIISW
3
A6
HIRES
2
A7
MIX
1
A8
TEXT
23
A9
V2
22
A10
V4
19
A11
+5
7
A2
6
A1
65
CS2 CS3 CS4
12
20
21
+5
D7
17
DHIRES
D6
16
AIILORES
D5
15
OE 374
D4
14
CH80
D3
13
AHIRES
D2
11
COLRKL
D1
10
SEL 374
D0
9
PG2
7
J20

PG2=AIISW'*(HIRES*MIX'*TEXT ')'*HIRES*PAGE2*S4*VBL'

SEL374=(VBL'*(AIISW*(PAGE2'*(TEXT +MIX*V2*V4)'+PAGE2*(TEXT +MIX*V2*V4))+ AIISW'*(HIRES*(PAGE2*S4)'+HIRES'*(PAGE2*S4))))'

COLRKL'=(AIISW*TEXT +AIISW'*(HIRES'*(MIX+TEXT ')+HIRES*TEXT '))'

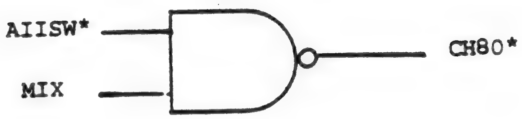
AHIRES=AIISW'*(HIRES*MIX*TEXT )

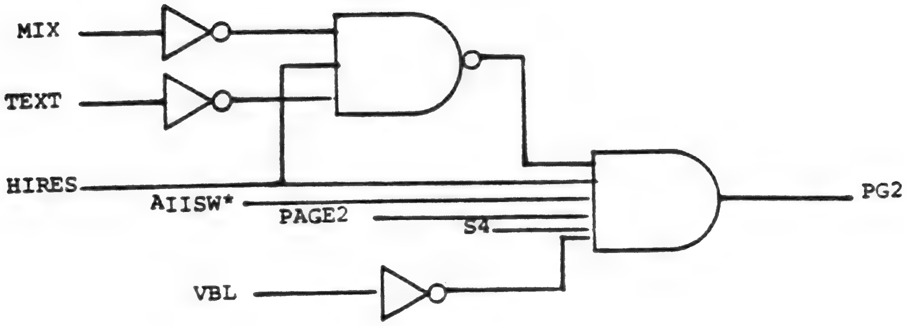
CH80'=(AIISW'*MIX)'

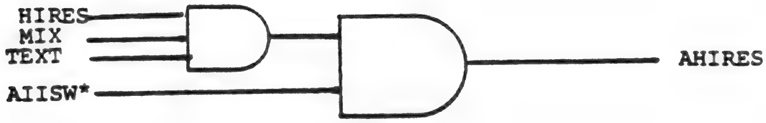
OE374=(AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*MIX'*TEXT )'

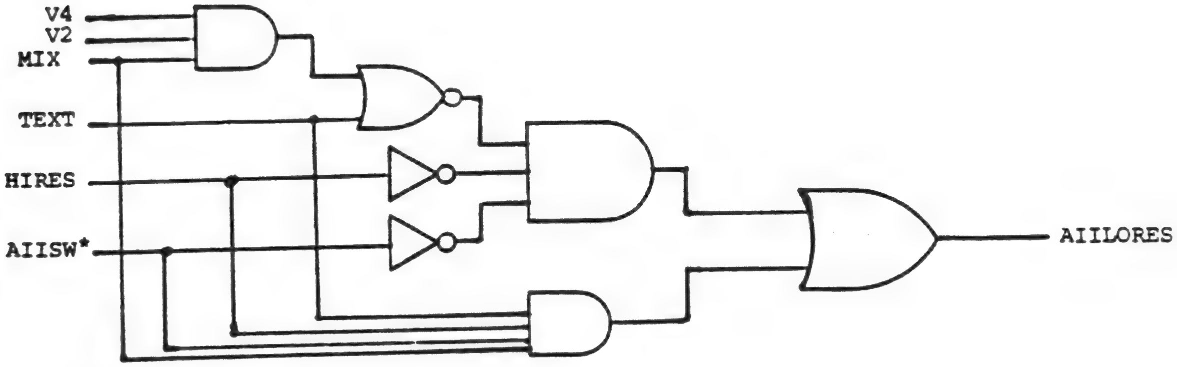
AIILORES=AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*HIRES*MIX*TEXT

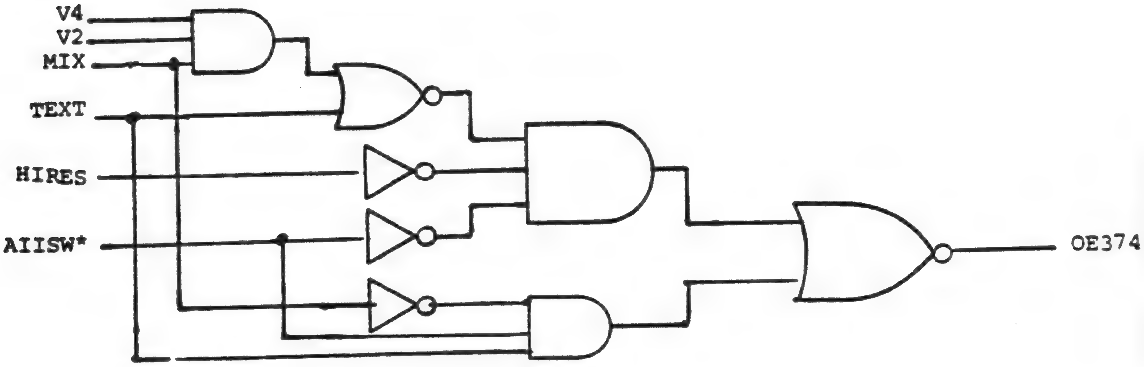
DHIRES=(AIISW*HIRES*(TEXT +MIX*V2*V4)'+AIISW'*HIRES)*VBL'


AIISW*
MIX
CH80*


MIX
TEXT
HIRES
AIISW*
PAGE2
S4
VBL
PG2


HIRES
MIX
TEXT
AIISW*
AHIRES


V4
V2
MIX
TEXT
HIRES
AIISW*
AIILORES


V4
V2
MIX
TEXT
HIRES
AIISW*
OE374

## THE COLOR VIDEO CONNECTOR

| Pin | Name | Description |
|---|---|---|
| 1 | SG | Shield Ground. |
| 2 | XRGB4 | One of four GRB outputs. This (and pins 5, 9, and 10) is a TTL output with instantaneous color information. A linear weighted sum of these four signals will form a true 16-color RGB video signal |
| 3 | SYNCH | Composite synchronization signal with negative-going tips. |
| 4 | PDI | Not used. |
| 5 | XRGB1 | See pin 2. |
| 6 | GND | Power and signal ground. |
| 7 | -5V | -5 volt power supply. A device may draw up to 200 ma through this pin. |
| 8 | +12V | +12 volt power supply. A device may draw up to 500 ma through this pin. |
| 9 | XRGB2 | See pin 2. |
| 10 | XRGB8 | See pin 2. |
| 11 | BWVID | Black and white composite video. This is an NTSC composite video signal with negative-going synch tips, 1 volt peak-to peak into a 75 ohm load. Color information is encoded as a linear grey scale. |
| 12 | NTSC | Color composite video. This is an NTSC-compatible video signal with negative-going sych tips, 1 volt peak-to-peak into a 75 ohm load. |
| 13 | GND | Power and signal ground. |
| 14 | -12V | -12 volt power supply. A device may draw up to 200 ma through this pin. |
| 15 | +5V | +5 volt supply. A device may draw up to 1 amp through this pin. |

This connector supplies 7 different video signals and 4 power supply voltages. Through this connector you can hook up the Apple to any NTSC color or black and white video monitor. With an additional circuit you can hook up the Apple to a studio-quality RGB color monitor.

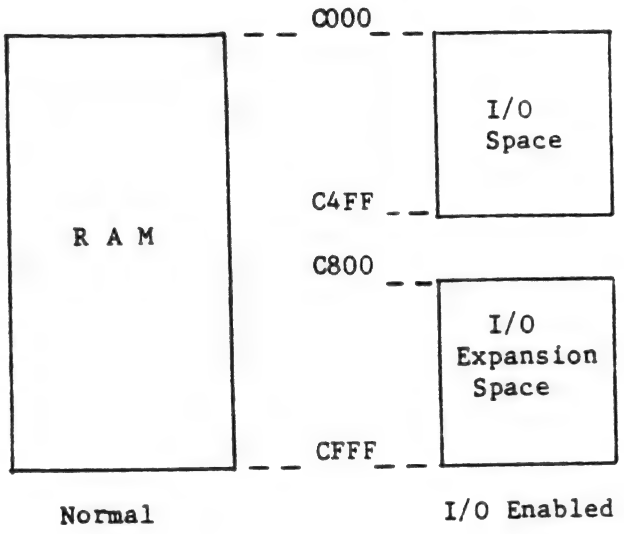
All power supply current ratings assume that no peripheral cards are installed in the system. If there are cards in the system, be sure to account for the current drawn by those cards.

# INPUT/OUTPUT (I/O)

## DESCRIPTION

In Apple computers I/O devices are treated very much like memory locations. Most of the system's I/O functions are mapped into the address range C000 to CFFF. The I/O space is enabled by a bit in the Environmental Register. Addresses C0XX control the on-board I/O. Addresses C1XX, C2XX, C3XX, and C4XX are reserved for the exclusive use of the four I/O slots. The I/O expansion space from C800 to CFFF is switched between the I/O slots. Addresses C500 to C7FF are always Ram, regardless of the setting of the I/O enable bit.

### I/O ADDRESS SPACE



## INTERFACE CONTROL SIGNALS

For every I/O slot, the Apple /// provides 16 locations that set the Device Select* signal and 256 locations that set the I/O Select* signal.

The Device Select* signal is a signal specific to each slot. It is active for for a 16-address block. This signal is ususally used as an enable signal.

The I/O Select* signal can be used to control a page of memory (256 addresses) which could be placed in ROM, in the interface circuitry, for executing "driver routines". The I/O Select* signal could also be used in circumstances where a small amount of read/write memory for temporary storage is needed. Each I/O slot has its own I/O Select* signal, and each signal is active when a specific page of memory is addressed.

The I/O Strobe is common to all I/O slots. This signal will be low (true) when an address location within the range of C800 to CFFF (2K of memory).

## INTERRUPTS

Interface cards that are capable of generating interrupts MUST latch the interrupt output until it is reset by the software. In addition, they MUST include the ability to mask and unmask their interrupt through software, and MUST default to the masked state when the system is reset.

| | |
|---|---|
| C09X | Slot 1 Device Select |
| C1XX | Slot 1 I/O Select |
| C0AX | Slot 2 Device Select |
| C2XX | Slot 2 I/O Select |
| C0BX | Slot 3 Device Select |
| C3XX | Slot 3 I/O Select |
| C0CX | Slot 4 Device Select |
| C4XX | Slot 4 I/O Select |

The method of accomplishing this transmission between the interface and the computer is called handshaking. In the Apple ///, the handshaking is normally accomplished through the exchange of Device Select*, I/O Select*, IRQ*, and R/W*. The R/W* control signal is used to synchronize the flow of data to and from I/O devices. When the Read/Write* signal is a logic one, the processor is reading information from the data bus. Conversely, when R/W* is low, we are performing a write to the data bus.

As you can see, the handshaking between the Apple /// and the interface is dependent upon the software. Let us again emphasize the role of addressing plays in the I/O process.

## ADDRESSING THE I/O

There are certain addresses that you can write to or read from to control the operation of the interface card. Where "n" is the number of the slot where the interface is installed, these hardware addresses are in the range:

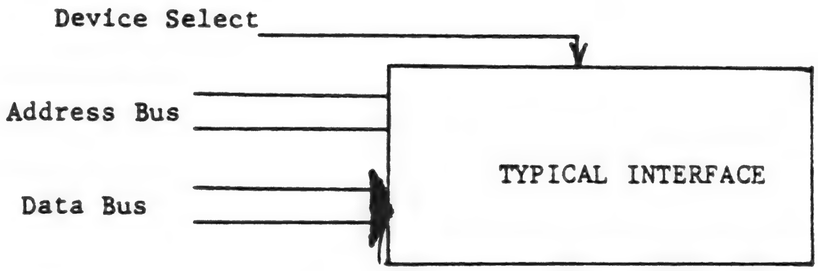
C080 + n0 to C087 + n0

For example, if you install an interface in slot 2, you should write to the addresses from C0A0 through C0A7.

The operations that the interface card performs are initiated by the read or write operations presented on these hardware addresses.

## THE INPUT OPERATION

In the input operation, whenever the correct address is presented to the interface card, the data is present on the data lines D7-D0. For example, if the location C083 + n0 corresponds in the software to an input, the data presented on D7-D0 is accepted by the computer. If the interface card contains a control ROM, the code in ROM is being addressed whenever the I/O Select line is low; that is when the address on the address lines is between Cn00 and CnFF). Recall that "n" is the slot number.

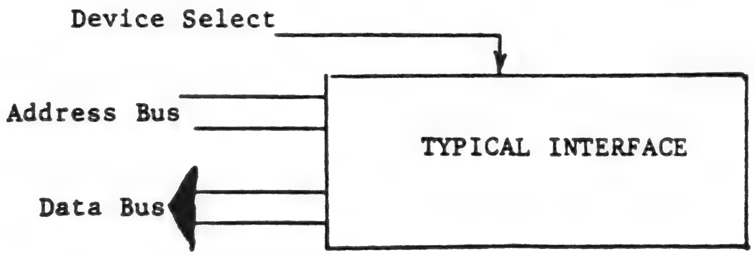

Device Select
Address Bus
Data Bus
TYPICAL INTERFACE

## THE OUTPUT OPERATION

In the output operation,

IF the address Co81 + n0 represents an output operation
in the software
AND the Read/Write* signal is low,

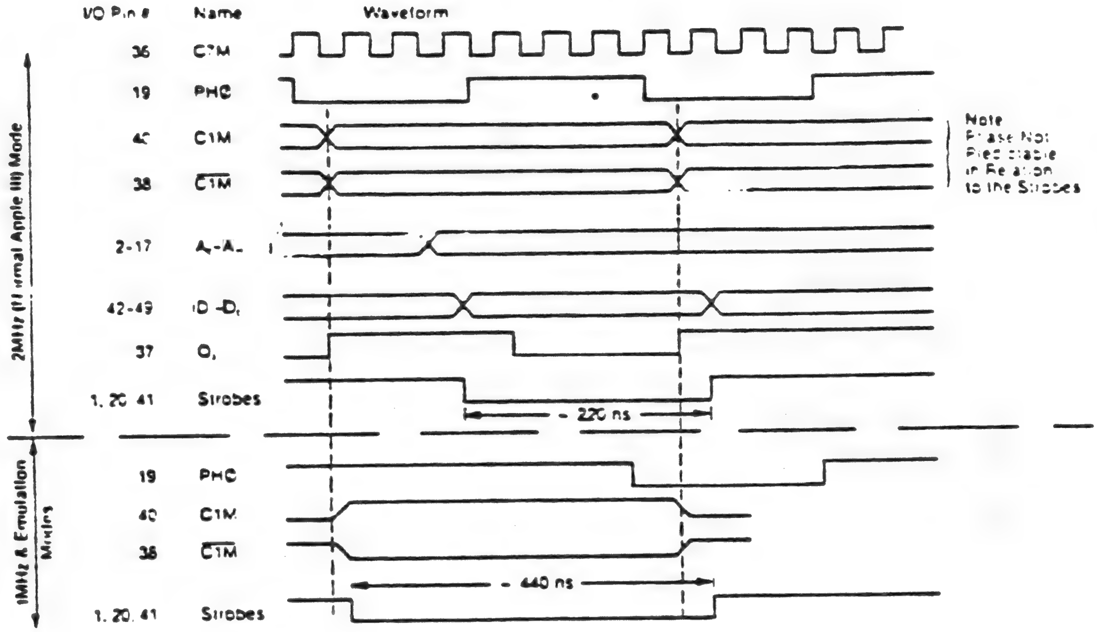
THEN the data is presented on the data bus and latched into
the interface whenever the address C081 + n0 is presented.


Device Select
Address Bus
Data Bus
TYPICAL INTERFACE

## SYSTEM TIMING

A system timing diagram is provided. This diagram shows the timing of some signals at the I/O slots in the 1 MHz and 2 MHz frequency modes.

# I/O TIMING DIAGRAMS


I/O Pin #
Name
Waveform
36
C7M
19
PHC
40
C1M
38
C1M
2-17
A0-A15
42-49
D0-D7
37
O1
1, 20, 41
Strobes
220 ns
Note
Phase Not
Predictable
in Relation
to the Strobes
2MHz (Normal Apple III) Mode
19
PHC
40
C1M
38
C1M
440 ns
1, 20, 41
Strobes
1MHz & Emulation Modes

## THE A/// JOYSTICK

The A/// has two ports designated for joystick (x and y axis paddles) each with two switches. However, unlike the Apple II the ports do not have "annunicator" outputs. One of the switches is a momentary contact and the other is a toggle.

The Analog X and Y inputs are read through a ramp type Analog to Digital converter (A/D). These values derived must be interpreted by the program. The switches are read to the data bus directly through a mulitplexor.

The 9708 has multiplexed inputs. To select which input channel is to be read the proper address must be set in an addressable latch and must be held during the PDLEN (ramp start) low cycle.

The I/O address for the setting and clearing of the A/D addresses and the ramp start is as shown in the following table:

| I/O Address | A/D Function | Signal Name |
|---|---|---|
| C058 | A0 Clear | PDL0 |
| C059 | A0 Set | |
| C05A | A2 Clear | PDL2 |
| C05B | A2 Set | |
| C05C | Ramp Start Clear | PDLEN |
| C05D | " " Set | |
| C05E | A1 Clear | AXC0 |
| C05F | A1 Set | |

To read the various signals associated with the joysticks the following addresses should be read:

| I/O Address | Function |
|---|---|
| C060,8 | Switch 0 |
| C061,9 | Switch 1/Margin Switch |
| C062,A | Switch 2 |
| C063,B | Switch 3/Serial Clock |
| C066,E | A/D ramp stop (PDLOT) |

Note: The joystick port at J3 (Port A) can be configured to be a serial port to support a device like-the Silentype. Care must be taken to insure that the port has been configured for the proper device or signal contention will occur and give erroneous results.

The sequence of operation for the A/D would be as follows:

1) set the desired channel address nto A/D 0 through A/D 2.

2) start the A/D by cycling the PDLEN signal low for 40 micro seconds then back high

3) set up one of the timers to count.

4) test for ramp stop

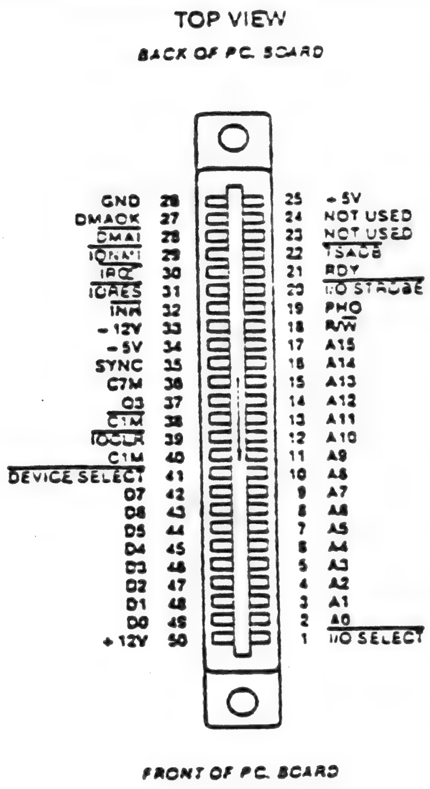
5) read the counter

6) compute the value of the channel input.

## Peripheral Connector Pinout

| | | | |
|---|---|---|---|
| GND | 26 | 25 | +5V |
| DMAOK | 27 | 24 | NOT USED |
| $\overline{\text{DMAI}}$ | 28 | 23 | NOT USED |
| $\overline{\text{IONMI}}$ | 29 | 22 | $\overline{\text{TSADE}}$ (Open collector) |
| $\overline{\text{IRQ}}$ | 30 | 21 | RDY (Open collector) |
| $\overline{\text{IORES}}$ | 31 | 20 | $\overline{\text{I/O STROBE}}$ |
| $\overline{\text{INH}}$ | 32 | 19 | PHO |
| -12V | 33 | 18 | R/$\overline{\text{W}}$ |
| -5V | 34 | 17 | A15 |
| SYNC | 35 | 16 | A14 |
| C7M | 36 | 15 | A13 |
| Q3 | 37 | 14 | A12 |
| $\overline{\text{C1M}}$ | 38 | 13 | A11 |
| $\overline{\text{IOCLR}}$ | 39 | 12 | A10 |
| C1M | 40 | 11 | A9 |
| $\overline{\text{DEV SEL}}$ | 41 | 10 | A8 |
| D7 | 42 | 9 | A7 |
| D6 | 43 | 8 | A6 |
| D5 | 44 | 7 | A5 |
| D4 | 45 | 6 | A4 |
| D3 | 46 | 5 | A3 |
| D2 | 47 | 4 | A2 |
| D1 | 48 | 3 | A1 |
| D0 | 49 | 2 | A0 |
| +12V | 50 | 1 | $\overline{\text{I/O SELECT}}$ |

A/// Peripheral Connector Slot


TOP VIEW
BACK OF P.C. BOARD
GND 26
DMAOK 27
DMAI 28
IONMI 29
IRQ 30
IORES 31
INH 32
-12V 33
-5V 34
SYNC 35
C7M 36
Q3 37
C1M 38
IOCLR 39
C1M 40
DEVICE SELECT 41
D7 42
D6 43
D5 44
D4 45
D3 46
D2 47
D1 48
D0 49
+12V 50
25 +5V
24 NOT USED
23 NOT USED
22 TSADE
21 RDY
20 I/O STROBE
19 PHO
18 R/W
17 A15
16 A14
15 A13
14 A12
13 A11
12 A10
11 A9
10 A8
9 A7
8 A6
7 A5
6 A4
5 A3
4 A2
3 A1
2 A0
1 I/O SELECT
FRONT OF P.C. BOARD

## Table 33: Peripheral Connector Signal Description

| Pin: | Name: | I/O | Description: |
|---|---|---|---|
| 1 | $\overline{\text{I/O SELECT}}$ | O | This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PH0 (nominally 500ns) and will drive 12 LSTTL loads. |
| 2-17 | A0-A15 | I, O | The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PH0. These lines will each drive 8 LSTTL loads. |
| 18 | R/$\overline{\text{W}}$ | I, O | Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads. |
| 19 | PH0 | O | A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs. |
| 20 | $\overline{\text{I/O STROBE}}$ | O | This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads. |
| 21 | RDY | I | The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output. |
| 22 | $\overline{\text{TSADB}}$ | I | A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output. |
| 23 |  | NA | Not used in an Apple ///(NO DAISY CHAINING OF PERIPHERALS) |
| 24 |  | NA | Not used in an Apple ///. |
| 25 | +5V | O | Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board). |
| 26 | GND | NA | System circuit ground. 0 volt line from power supply. Do not use for shield ground. |
| 27 | DMAOK | O | Acknowledge signal to the peripheral following |

| | | | |
|---|---|---|---|
| | | | its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed. |
| 28 | DMAI | I | Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output. |
| 29 | IONMI | I | Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output.<br>THE NMI DOES NOT GO DIRECTLY T THE PROCESSOR, SO IT CAN BE MASKED BY THE SYSTEM RESET FUNCTI |
| 30 | IRQ | I | This line is ignored in Apple ][ emulation mode. It should be driven by a TTL output. |
| 31 | IORES | O | Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads. |
| 32 | INH | I | Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output. |
| 33 | -12V | O | Negative 12 volt supply, 200mA total for all peripheral boards together. |
| 34 | -5V | O | Negative 5 volt supply, 200mA total for all periperal boards together. |
| 35 | SYNC | O | The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads. |
| 36 | C7M | O | Seven MHz high frequency clock. Will drive 10 LSTTL loads. |
| 37 | Q3 | O | A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs. |
| 38 | C1M | O | Complement of C1M clock. This will drive 12 LSTTL loads. |
| 39 | IOCLR | O | Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple ][ peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads. |
| 40 | C1M | O | Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads. |
| 41 | DEVICE SELECT | | This line becomes acive (low) on each peripheral |

| | | | |
|---|---|---|---|
| | | | connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads. |
| 42-49 | D7-D0 | I,O | The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{\text{C1M}}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{\text{C1M}}$. These lines will drive 8 LSTTL inputs. |
| 50 | +12V | O | Positive 12 volt supply*, 300mA total for all peripheral boards together. |

* NOTE: TOTAL POWER DRAWN BY ANY ONE PERIPHERAL BOARD IS NOT TO EXCEED 1.5 WATTS

## The Real Time Clock/Calendar

A real time clock has been incorporated into the A /// using 58167 CMOS Clock/Calendar chip. This chip has the resolution to count to thousandths of a second. The clock circuitry can be set to cause an interrupt at intervals from a tenth of a second to interrupts every month.

Since the clock is a CMOS circuit it consumes about 10ua in the standby (power off in the Apple ///) mode. This is about the same as a normal LCD watch. Three "AA" alkaline batteries are mounted in a battery pack that clips to the casting near the internal speaker. Wires attached to the battery holder connect to a 2 pin molex connector at location G13.

This clock chip is not a member of the 6500 family and is not directly compatible. Special considerations have been incorporated into the logic design to allow the Apple III to access and control of the clock chip.

The timing requirements for the clock chip require that the address lines be latched for much longer than the processor can accomplish in normal operations, so the clock is addressed with the "Zero Page Register" (the B port of VIA B6). The operating system will temporarily store the current zero page address at another location then write the desired clock address into the zpage register. The processor clock, PHO, is extended to --usec by the action of the prom 180 and associated circuit. The clock chip also requires a separate read and write strobe so appropriate logic was designed to split the R/W signal into a read and write strobe.

When the processor has completed its access to the clock it will return the proper zero page address to the VIA and PHO will return to its normal operation.

Please refer to the specification sheet in the Appendices for complete details of the clock.

The transistor array performs two functions. One it supplies Vcc from the power supply when the Apple /// is "on", and develops a power down strobe to the clock chip to set its standby mode just before the supply fully decays.

The clock may be programmed that while it is in the standby mode to provide a PDINT to an external device which may restore power to the Apple to service a particular device. This feature would be very useful in communications networks that poll at specific times in off-hours. However, at the time of this printing no such remote device has been specified.

The clock runs on a 32KHZ crystal may be adjusted to an operating tolerance of 5 minutes a month. There are two methods used, on is a vertifications of operation using software, this however has the accuracy of approximately 5 minutes a month, which for many applications and users is close enough, but for those users who demand a closer setting a method of setting the clock using an accoustic probe and frequently meter is available. The only problem with this is the cost of the calibration equipment (nearly $1000 per station). Level II centers will most likely be equipped with these devices.

It should be noted that there is a slight shift if frequently between power on and standy modes. Depending on the actual usage of power on and off the clock may vary perceptibly over the course of a month. So it is best to describe the entire function as a clock, not a chronograph.

# THE KEYBOARD

The Apple /// has a built-in 74 key typewriter-like keyboard which includes full alpha/numerics, four cursor control keys, two special function keys, and a numeric keypad. It has full upper and lower case ASCII code generation capability as well as full incorporation of Apple ][ functions.

The drawing on the previous page shows the standard keyboard legend and details the keystation number. Note that in addition to the 74 keys there is a recessed Reset key. Every key on the keyboard can be observed individually by the soft- ware. The Control and Shift keys modify the key codes when presented to the system.

The keyboard is electrically connected to the main circuit board by a 26 conductor ribbon cable. The cable plugs into a socket on the keyboard and the main circuit board. The signal assignment is shown on the Pin Signal Assignment table.

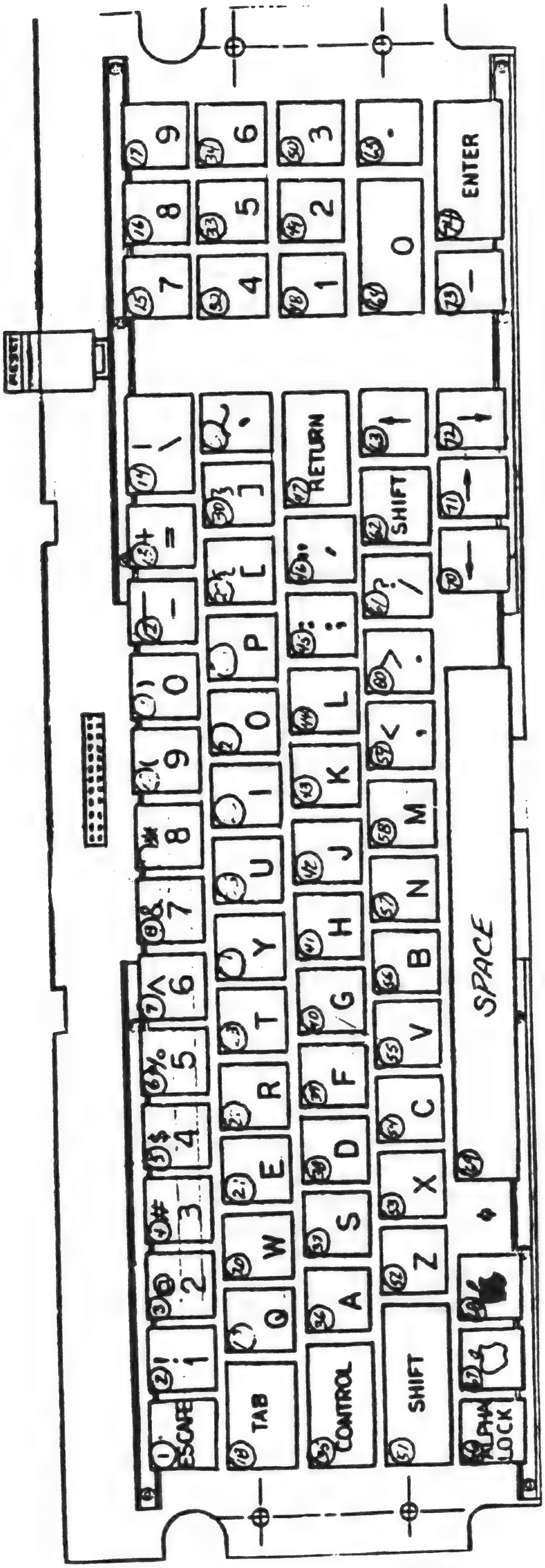
## Repeat Functions

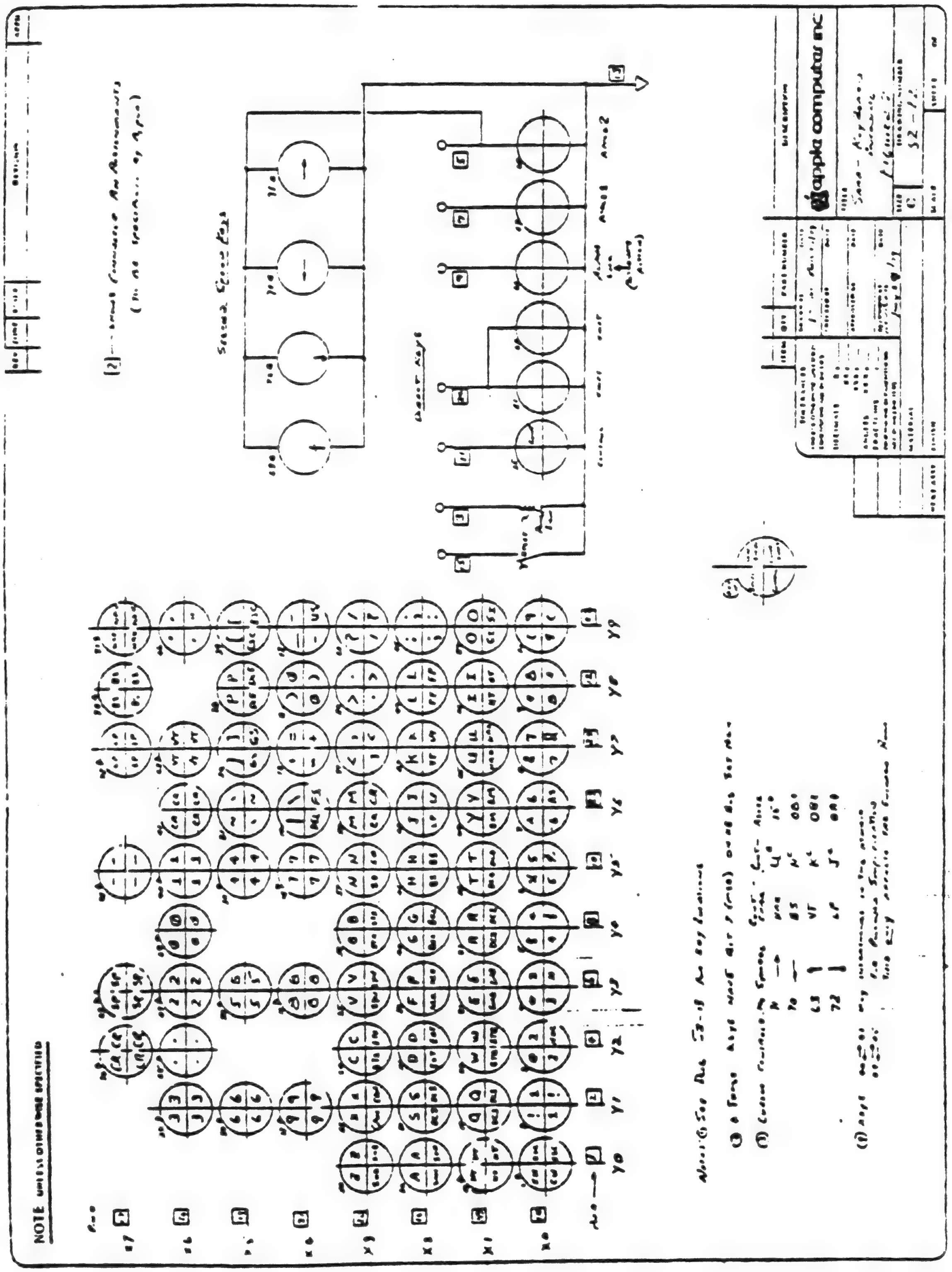
Any key held down for more thn 1/2 second is automatically activated to repeat at a 10 CPS rate. A high speed (30 CPS) repeat function is activated by holding down the closed Apple key (Key #68) after depressing and holding the key to be repeated. An idiosyncracy of the Apple /// is that if the closed Apple key is depressed before another key, it is displayed as only one character. If it is depressed after another key, the high speed repeat is activated.

The four cursor control keys (63, 70, 71, 72) are two-contact keys. This means that as the key is partially depressed, it makes its first contact generating a signal code. When it is fully depressed, it will make a second contact, automatically activating a high speed repeat of that key.

## READING THE KEYBOARD

The keyboard can be thought of as two hardware ports (busses) that can provide two distinct types of data. The first type is ASCII, which is addressed by Memory Address C000; we will call this the KA port. The KA port always contains the lower 7 bits of the ASCII code and, like the Apple ][, uses the MSB as a "keyboard data ready" flag. The second type of data is addressed by Memory Address C008; we call this the KB port. The KB port looks at the "direct connect" keys and at the eighth bit of the key code. A summary of the bit meanings for these two types of data is shown in the table at the top of the following page.


ESCAPE
TAB
CONTROL
SHIFT
ALPHA LOCK
SPACE
RETURN
SHIFT
ENTER
1 2 3 4 5 6 7 8 9 0
Q W E R T Y U I O P
A S D F G H J K L
Z X C V B N M


NOTE UNLESS OTHERWISE SPECIFIED
X7
X6
X5
X4
X3
X2
X1
X0
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
apple computer inc
C
52-12

## KEYBOARD ENCODER MATRIX

| | KEYBOARD | VERTICAL | Y | | | | | KEY PAD |
|---|---|---|---|---|---|---|---|---|
| Y0 | A | Z | ESC | TAB | | | | NONE |
| Y1 | 1 | Q | S | X | | | | 9 6 3 |
| Y2 | 2 | W | D | C | | | | . ENTER |
| Y3 | 3 | E | F | V | SPACE | | | 8 5 2 |
| Y4 | 4 | R | H | B | | | | 0 |
| Y5 | 5 | T | G | N | | | | 7 4 1 - |
| Y6 | 6 | \|<br>\ | Y | ~<br>\ | J | M | RETURN | NONE |
| Y7 | 7 | += | U | } ] | K | <, | ↑ ↓ | NONE |
| Y8 | 8 | 0 | I | P | ; : | ← | > . | NONE |
| Y9 | | 9 | §[ | 0 | " ' | L | ?/ | NONE |

| | KEYBOARD | HORIZONTAL X | | | | | | | | | KEY PAD |
|---|---|---|---|---|---|---|---|---|---|---|---|
| X0 | ESC | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | NONE |
| X1 | TAB | Q | W | E | R | T | Y | U | I | O | NONE |
| X2 | A | S | D | F | G | H | J | K | L | : ; | NONE |
| X3 | Z | X | C | V | B | N | M | <, | >. | ? / | NONE |
| X4 | 0 | ‾<br>- | + | = | \|<br>\ | | | | | | 7 8 9 |
| X5 | P | {<br>[ | }<br>] | ~<br>\ | | | | | | | 4 5 6 |
| X6 | " ' | RETURN | ↑ | | | | | | | | 1 2 3 . 0 |
| X7 | SPACE | ← | → | ↓ | | | | | | | - ENTER |

********************************************************************************

## MEMORY ADDRESS REFERENCE

********************************************************************************

| | KA PORT (C000) | | | KA PORT (C008) |
|---|---|---|---|---|
| Bit 0 | ASCII Bit 0 | * | Bit 0 | "1"="any key down" |
| Bit 1 | ASCII Bit 1 | * | Bit 1 | "0"="shift depressed" |
| Bit 2 | ASCII Bit 2 | * | Bit 2 | "0"="control depressed" |
| Bit 3 | ASCII Bit 3 | * | Bit 3 | "0"="alpha lock set" |
| Bit 4 | ASCII Bit 4 | * | Bit 4 | "0"="Apple 1 switch depressed" |
| Bit 5 | ASCII Bit 5 | * | Bit 5 | "0"="Apple 2 switch depressed" |
| Bit 6 | ASCII Bit 6 | * | Bit 6 | "1"="start up uncommitted mode" |
| Bit 7 | "1"="data ready flag" | * | Bit 7 | ASCII Bit 7 |

********************************************************************************

The KA data is used exactly like that in the Apple ][ keyboard. The KB data is provided for function expansion. The KB ports 1 to 5 are direct mechanical connections to defined function switches. Bit 0 is an output from the encoder circuity and bit 7 is the eighth bit of the key code. Bit 6 is a special bit, a flag used during turn-on to show that the operational mode (Apple /// or Apple ][) has not yet been determined..

It should be noted that the Reset key cannot act on its own but has to be depressed with another key. This is a safety feature to prevent blowing away a good night´s programming effort. Now isn´t that nifty!? A CONTROL- RESET will give a true system reset. However, it cannot be used for recovery from Apple ][ mode. The CONTROL-RESET will also give the system an NMI (Non-Maskable Interrupt). This provides Apple /// with two levels of "reset."

KEYBOARD CODES

A complete list of the codes generated by the encoder circuitry is presented is the following table:

Table: Apple /// KEYBOARD CODES (HEX)

| Key # | Key Name | US | SH | CT | SU-CT |
|---|---|---|---|---|---|
| 1* | ESCAPE | 9B | 9B | 9B | 9B |
| 2 | 1 | 31 | 21 | 31 | 31 |
| 3 | 2 | 32 | 40 | 32 | 00 |
| 4 | 3 | 33 | 23 | 33 | 23 |
| 5 | 4 | 34 | 24 | 34 | 24 |
| 6 | 5 | 35 | 25 | 35 | 25 |
| 7 | 6 | 36 | 5E | 36 | 53 |
| 8 | 7 | 37 | 26 | 37 | 26 |
| 9 | 8 | 38 | 2A | 38 | 2A |
| 10 | 9 | 39 | 28 | 39 | 28 |
| 11 | 0 | 30 | 29 | 30 | 29 |
| 12 | - | 2D | 5F | 2D | 1F |
| 13 | = | 3D | 2B | 3D | 2B |
| 14 | BACKLASH | 5C | 7C | 7F | 1C |
| 15* | 7 | B7 | B7 | B7 | B7 |
| 16* | 8 | B8 | B8 | B8 | B8 |
| 17* | 9 | B9 | B9 | B9 | B9 |
| 18* | TAB | 89 | 89 | 89 | 89 |
| 19 | Q | 51 | 51 | 11 | 11 |
| 20 | W | 57 | 57 | 17 | 17 |
| 21 | E | 45 | 45 | 05 | 05 |
| 22 | R | 52 | 52 | 12 | 12 |
| 23 | T | 54 | 54 | 14 | 14 |
| 24 | Y | 59 | 59 | 19 | 19 |
| 25 | U | 55 | 55 | 15 | 15 |
| 26 | I | 49 | 49 | 09 | 09 |
| 27 | O | 4F | 4F | 0F | 0F |
| 28 | P | 50 | 50 | 10 | 10 |
| 29 | RT-BRACK | 5B | 7B | 1B | 1B |
| 30 | LT-BRACK | 5D | 7D | 1D | 1D |
| 31 | LT-BRACK | 60 | 7E | 60 | 7E |
| 32* | 4 | B4 | B4 | B4 | B4 |
| 33* | 5 | B5 | B5 | B5 | B5 |
| 34* | 6 | B6 | B6 | B6 | B6 |
| 35 | CONTROL | -----KB-2------ | | | |
| 36 | A | 41 | 41 | 01 | 01 |
| 37 | S | 53 | 53 | 13 | 13 |
| 38 | D | 44 | 44 | 04 | 04 |

| Key # | Key Name | US | SH | CT | SU-CT |
|---|---|---|---|---|---|
| 39 | F | 46 | 46 | 04 | 04 |
| 40 | G | 47 | 47 | 07 | 07 |
| 41 | H | 48 | 48 | 08 | 08 |
| 42 | J | 4A | 4A | 0A | 0A |
| 43 | K | 4B | 4B | 0B | 0B |
| 44 | L | 4C | 4C | 0C | 0C |
| 45 | ; | 3B | 3A | 3B | 3A |
| 46 | ' | 27 | 22 | 27 | 22 |
| 47 | RETURN | 0D | 0D | 0D | 0D |
| 48* | 1 | B1 | B1 | B1 | B1 |
| 49* | 2 | B2 | B2 | B2 | B2 |
| 50* | 3 | B3 | B3 | B3 | B3 |
| 51 | SHIFT | -----KB-1------ | | | |
| 52 | Z | 5A | 5A | 1A | 1A |
| 53 | X | 58 | 58 | 18 | 18 |
| 54 | C | 43 | 43 | 03 | 03 |
| 55 | V | 56 | 56 | 16 | 16 |
| 56 | B | 42 | 42 | 02 | 02 |
| 57 | N | 4E | 4E | 0E | 0E |
| 58 | M | 4D | 4D | 0D | 0D |
| 59 | , | 2C | 3C | 2C | 3C |
| 60 | . | 2E | 3E | 2E | 3E |
| 61 | / | 2F | 3F | 2F | 3F |
| 62 | SHIFT | -----KB-1------- | | | |
| 63* | UP-CURSOR | 8B | 8B | 8B | 8B |
| 64* | 0 | B0 | B0 | B0 | B0 |
| 65* | . | AE | AE | AE | AE |
| 66 | ALPHA-LK | -----KB-3------ | | | |
| 67 | APPLE 1 | -----KB-4------ | | | |
| 68 | APPLE 2 | -----KB-5------ | | | |
| 69* | SPACE | A0 | A0 | A0 | A0 |
| 70* | LT-CURSOR | 8B | 8B | 8B | 8B |
| 71* | RT-CURSOR | 95 | 95 | 95 | 95 |
| 72* | DN-CURSOR | 8A | 8A | 8A | 8A |
| 73* | - | AD | AD | AD | AD |
| 74* | ENTER | 8D | 8D | 8D | 8D |

* Bit 7 (MSB) on these keys appears on bit 7 of KB port, on the KA port.

Note: the keys on the numeric keypad have only one code. Shift and Control have no effect on these keys.

## THE APPLE II EMULATION MODE

In this mode the Apple /// special functions are locked out, making the keyboard look exactly like the Apple ][. Thus, the Apple ][ software does not look at the KB port and must get all the Apple ][ codes for the KA port. This is the reason for coding and bit arrangements. However, the Apple /// functions are not really locked out and could be read by an enterprising programmer, if desired.

Some of the keyboard codings which should be noted because of the Apple II emulation mode are:

1. "NUL" is a control-@ (Control-Shift-2). With the Apple ][, the "NUL" is a Control-Shift-p.
2. "RS", record separator, is a control-Shift-6, which corresponds to control-Shift-n in the Apple ][.
3. The Shift-m, for a left square bracket in the japple ][, is not available in the emulation mode since the character is represented on the keyboard. The "GS", group separator, is a Control-left bracket rather than the Control-Shift-m.
4. "BS", backspace, has been retained for the left arrow and "NAK", negative acknowledgment, for the right arrow for both the Apple ][ and Apple /// modes.
5. "VT", vertical tab, and "LF, line feed, were chosen for the up and down cursor keys. In the Apple ][ mode these will not give a cursor movement (unless the operating system is changed) but will give the Control-k and Control-j codes. This could cause some slight confusion for those Apple ][ programs that use those codes (...now he tells me!).
6. The autorepeat and high speed repeat functions will work for the Apple ][ just like they do in the Apple /// mode. Nice!

## ELECTRONIC CIRCUIT DESCRIPTION

Please refer to sheet 9 of 10 of the Schematic (Drawing Number 050-0039) for the following Keyboard Logic circuit description.

The Apple /// keyboard is simply an 8 by 10 X,Y matrix which is scanned by the encoder circuit [keyboard encoder rom H14] on the main logic board. All keys are scanned with the exception of five keys [shift, control, capslock, Apple1, Apple2] that are direct connected. The second contacts of the cursor keys (high speed repeat function are OR´d wired into the Apple2 switch line on KB-5.

On the main board the encoder scans the keyboard matrix and provides the correct code outputs plus a strobe and an "any key down" signal. A diagram for the key matrix shows the key locations, and their ASCII character representations are shown on the following page. The special function keys can be detected separately from the standard control keys by observing that the MSB of the KB port is set high.

The A3 signal to the Tri-state data selectors (LS257's) selects whether the output of the LS257 will be a KA or KB port. If A3 is high, selected by memory address C008, the KB port is selected. The KBD line enable the reading of data off the keyboard.

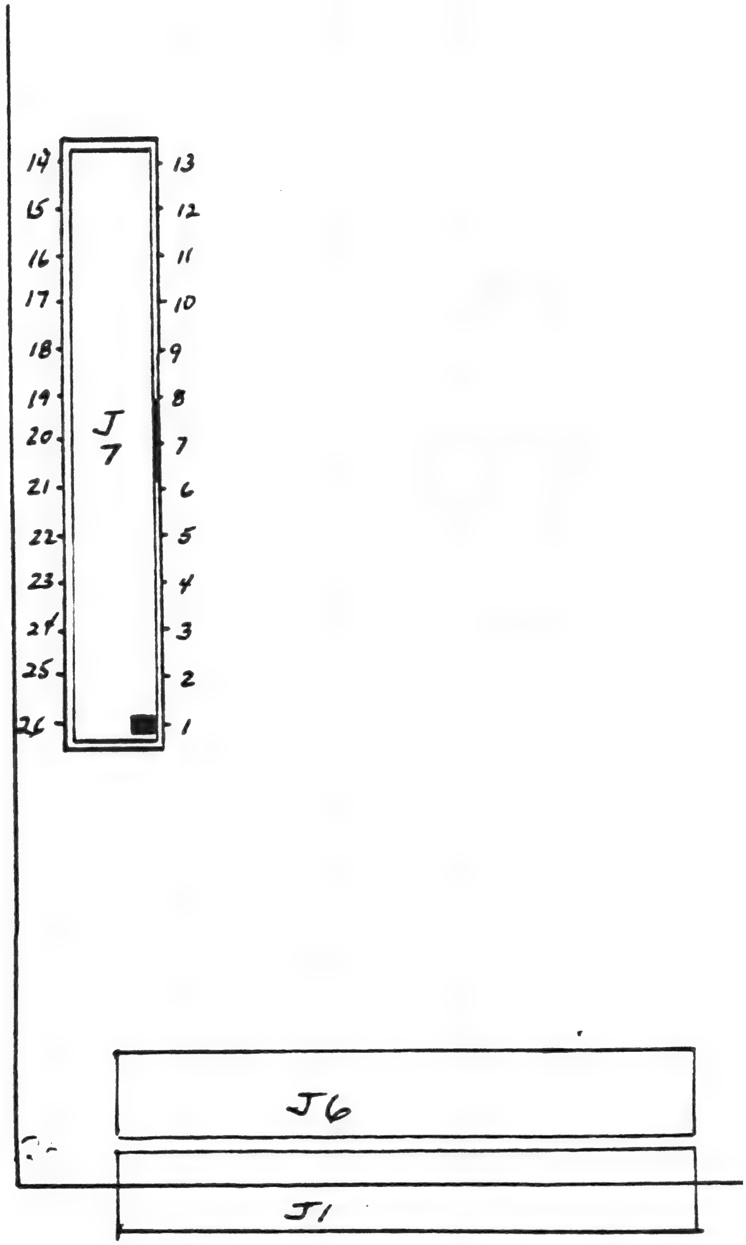
The Repeat Function: The normal repeat function (10 cps) that occurs when a key is held down is the result of clocking and resetting the flip-flop H11 (feeding into H12). This is accomplished by the AK (any key) and DTRDY (data ready) setting, H11 then having CLRSTB (clear strobe) resetting the flip-flop. The Apple2 key, when depressed after a character key, engages the high-speed repeat function. The combination of the Apple2 key signal clocking the edge triggered flip-flop (H11), and pulse change to the inputs of the 556 (L10) dual timers speeds up the timing.

The Reset Function: The power on reset is provided by the one shot (A5). Depressing the reset key results in a soft reset. This causes the KRESET line to go low and enable the LS139 (J11). If the Control key and the Reset key are both depressed, a hard reset results. This hard reset can be foiled through sophisticated programming. The RESETLK (reset lock signal) provided from the Environmental Register [6522 - B6], can disable the Reset and NMI. (Try it!)

Keyboard Light: The keyboard light indicates the VCC is provided to the keyboard. If no light is observed, check Q9 [MPV 51].

# PIN SIGNAL ASSIGNMENT

| Pin # | Description |
|---|---|
| 1 | Y0 |
| 2 | Y1 |
| 3 | Power Light |
| 4 | Y2 |
| 5 | Apple 2 (high speed repeat) |
| 6 | Y3 |
| 7 | Apple 1 |
| 8 | Y4 |
| 9 | Alpha Lock (alternate action) |
| 10 | Y5 |
| 11 | Control |
| 12 | Y8 |
| 13 | Signal Ground |
| 14 | X0 |
| 15 | Reset |
| 16 | X2 |
| 17 | X7 |
| 18 | X2 |
| 19 | X5 |
| 20 | X3 |
| 21 | X4 |
| 22 | Y9 |
| 23 | Y6 |
| 24 | Shift (both keys) |
| 25 | Y7 |
| 26 | X6 |

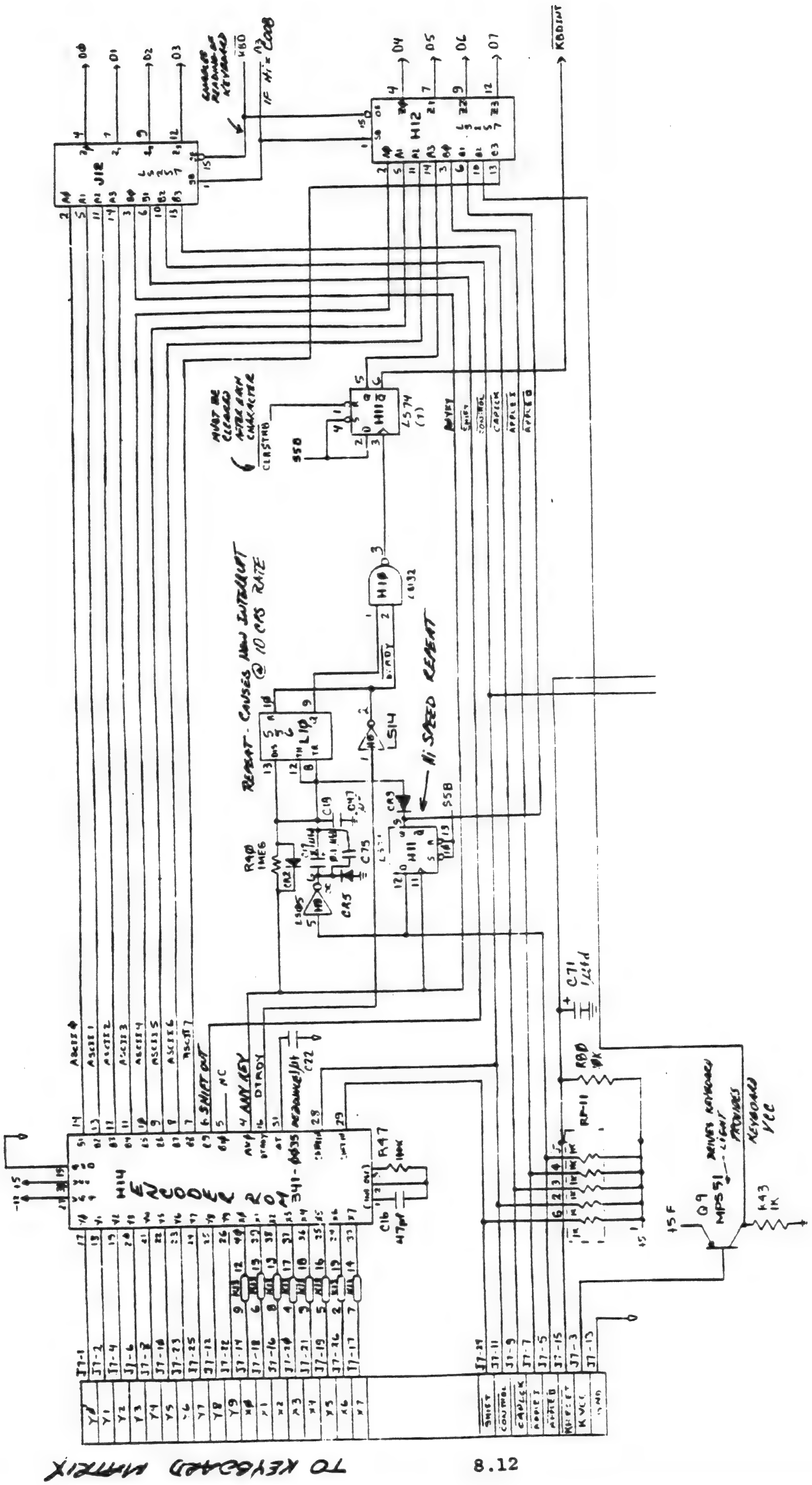

14
15
16
17
18
19
20
21
22
23
24
25
26
13
12
11
10
9
8
7
6
5
4
3
2
1
J7
J6
J1

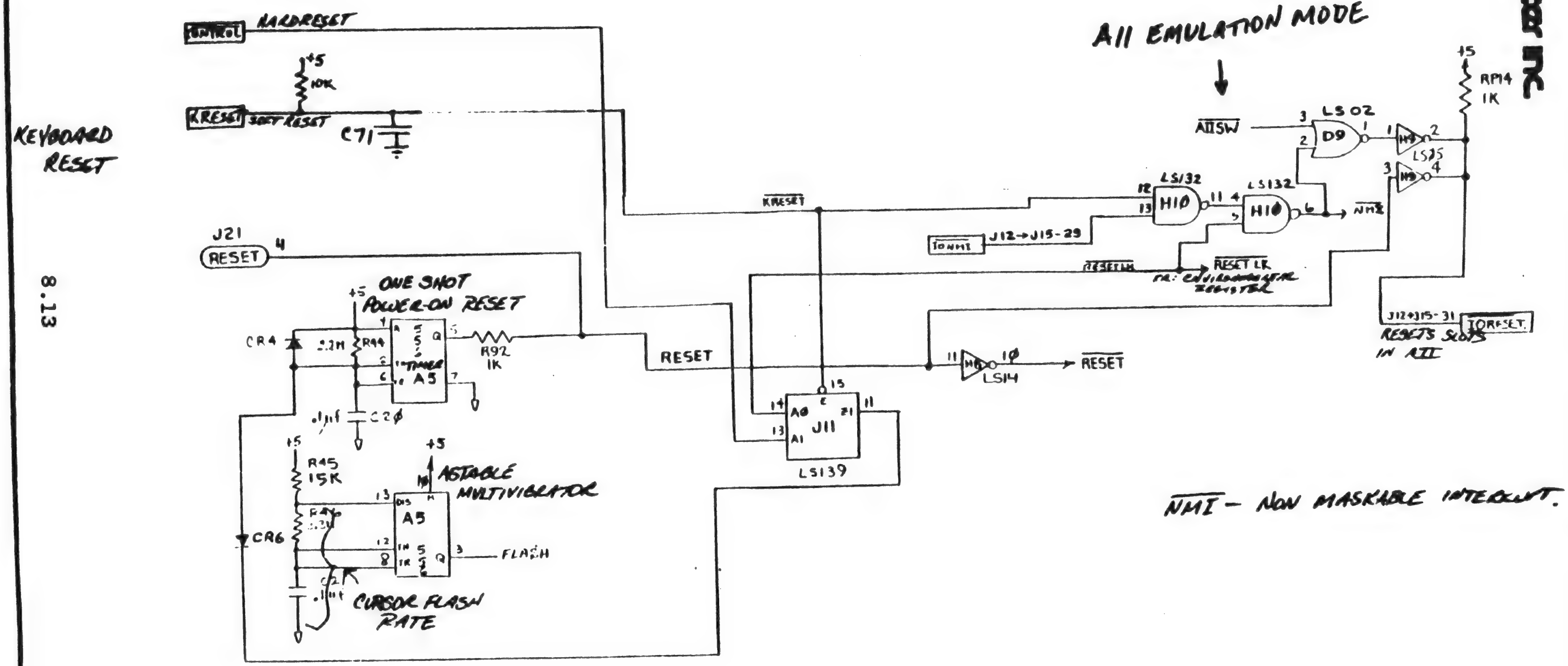
$ = REPRESENTS HEXADECIMAL

Table 2: Keys and their Associated ASCII Codes (Bit 7 always set)

| Key | Alone | CONTROL | SHIFT | Both |
|---|---|---|---|---|
| <space> | $A0 | $A0 | $A0 | $A0 |
| ESCAPE | $9B | $9B | $9B | $9B |
| 1! | $B1 | $B1 | $A1 | $A1 |
| 2@ | $B2 | $B2 | $C0 | $80 |
| 3# | $B3 | $B3 | $A3 | $A3 |
| 4$ | $B4 | $B4 | $A4 | $A4 |
| 5% | $B5 | $B5 | $A5 | $A5 |
| 6^ | $B6 | $B6 | $DE | $9E |
| 7& | $B7 | $B7 | $A6 | $A6 |
| 8* | $B8 | $B8 | $AA | $AA |
| 9( | $B9 | $B9 | $A8 | $A8 |
| 0) | $B0 | $B0 | $A9 | $A9 |
| -_ | $AD | $AD | $DF | $9F |
| =+ | $BD | $BD | $AB | $AB |
| \\| | $DC | $9C | $FC | $FF |
| TAB | $89 | $89 | $89 | $89 |
| [{ | $DB | $9B | $FB | $9B |
| ]} | $DD | $9D | $FD | $9D |
| '" | $A7 | $A7 | $A2 | $A2 |
| RETURN | $8D | $8D | $8D | $8D |
| ,< | $AC | $AC | $BC | $BC |
| .> | $AE | $AE | $BE | $BE |
| /? | $AF | $AF | $BF | $BF |
| <left arrow> | $88 | $88 | $88 | $88 |
| <right arrow> | $95 | $95 | $95 | $95 |
| <up arrow> | $8B | $8B | $8B | $8B |
| <down arrow> | $8A | $8A | $8A | $8A |
| . | $AE | $AE | $AE | $AE |
| - | $AD | $AD | $AD | $AD |
| ENTER | $8D | $8D | $8D | $8D |
| A | $C1 | $81 | $C1 | $81 |
| B | $C2 | $82 | $C2 | $82 |
| C | $C3 | $83 | $C3 | $83 |
| D | $C4 | $84 | $C4 | $84 |
| E | $C5 | $85 | $C5 | $85 |
| F | $C6 | $86 | $C6 | $86 |
| G | $C7 | $87 | $C7 | $87 |
| H | $C8 | $88 | $C8 | $88 |
| I | $C9 | $89 | $C9 | $89 |
| J | $CA | $8A | $CA | $8A |
| K | $CB | $8B | $CB | $8B |
| L | $CC | $8C | $CC | $8C |
| M | $CD | $8D | $CD | $8D |
| N | $CE | $8E | $CE | $8E |
| O | $CF | $8F | $CF | $8F |
| P | $D0 | $90 | $D0 | $90 |
| Q | $D1 | $91 | $D1 | $91 |
| R | $D2 | $92 | $D2 | $92 |
| S | $D3 | $93 | $D3 | $93 |
| T | $D4 | $94 | $D4 | $94 |

|  |  |  |  |  |
|---|---|---|---|---|
| U | $D5 | $95 | $D5 | $95 |
| V | $D6 | $96 | $D6 | $96 |
| W | $D7 | $97 | $D7 | $97 |
| X | $D8 | $98 | $D8 | $98 |
| Y | $D9 | $99 | $D9 | $99 |
| Z | $DA | $9A | $DA | $9A |


D0
D1
D2
D3
D4
D5
D6
D7
KBDINT
ENABLES READING OF KEYBOARD
KBD
IF Hi = C008
J12
H12
H11
LS74
MUST BE CLEARED AFTER EACH CHARACTER
CLRSTRB
SSB
ANYKEY
SHIFT
CONTROL
CAPLCK
APPLE 1
APPLE 0
REPEAT - CAUSES NEW INTERRUPT @ 10 CPS RATE
H10
LS132
DTRDY
L10
LS14
Hi SPEED REPEAT
R40
1MEG
CR2
CR5
CR3
C19
C75
C47
LS05
C71
1.0uf
R80
10K
RP-11
DRIVES KEYBOARD LIGHT
PROVIDES KEYBOARD VCC
Q9
MPS51
R43
1K
+5F
ASCII 0
ASCII 1
ASCII 2
ASCII 3
ASCII 4
ASCII 5
ASCII 6
ASCII 7
SHIFT OUT
NC
ANY KEY
DTRDY
C22
H14
ENCODER ROM
341-0035
R47
100K
C16
47pf
-12
+5
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
X0
X1
X2
X3
X4
X5
X6
X7
KVCC
GND
TO KEYBOARD MATRIX


A II EMULATION MODE
KEYBOARD RESET
CONTROL
HARDRESET
+5
10K
KRESET
SOFT RESET
C71
J21
RESET
4
ONE SHOT
POWER-ON RESET
+5
CR4
2.2M
R44
TIMER
A5
R92
1K
.1μf
C20
+5
R45
15K
ASTABLE
MULTIVIBRATOR
R46
3.3M
CR6
A5
FLASH
C21
.1μf
CURSOR FLASH RATE
RESET
KRESET
LS139
J11
A0
A1
E
14
13
15
11
LS14
H6
11
10
RESET
IONMI
J12→J15-29
RESETLM
RESET LR
FR: ENVIRONMENTAL REGISTER
LS132
H10
12
13
11
4
5
6
NMI
A2SW
LS02
D9
3
2
1
LS05
H9
1
2
3
4
+5
RP14
1K
J12→J15-31
IORESET
RESETS SLOTS IN AII

$\overline{NMI}$ - NON MASKABLE INTERRUPT.

# RESET

## THE APPLE /// POWER SUPPLY

The Apple /// power supply converts power from the AC line to DC. This is a constant voltage power supply. This means:

1. The output voltage is maintained constant regardless of changes in the load, line, or temperature.

2. The Apple /// power supply is a free running flyback type, off line switching power supply.

    - It can accept either 115VAC or 230VAC (jumper selectable) and delivers 4 regulated DC outputs at a total of 55 watts.

    - It supplies +5, -5, +11.8, and -12VDC.

    - It is called a flyback type power supply because energy is transferred from the primary of the transformer to the secondary when the switching transistor switches off (during flyback).

The following paragraphs will describe the switching power supply in more detail.

## THE BASIC SWITCHING POWER SUPPLY

The regulating element of the switching power supply consists of a transistor that acts as a rapidly opened and closed switch. The AC input is rectified to unregulated DC, then "chopped" by the switching element components at a fast rate, approximately 25kHz. The resultant is transformer-coupled to an output network which provides the final rectification and filtering. Regulation is accomplished through control circuits that vary the on-off periods (duty cycles) of the switching components.

### Advantages

1. Greater Efficiency

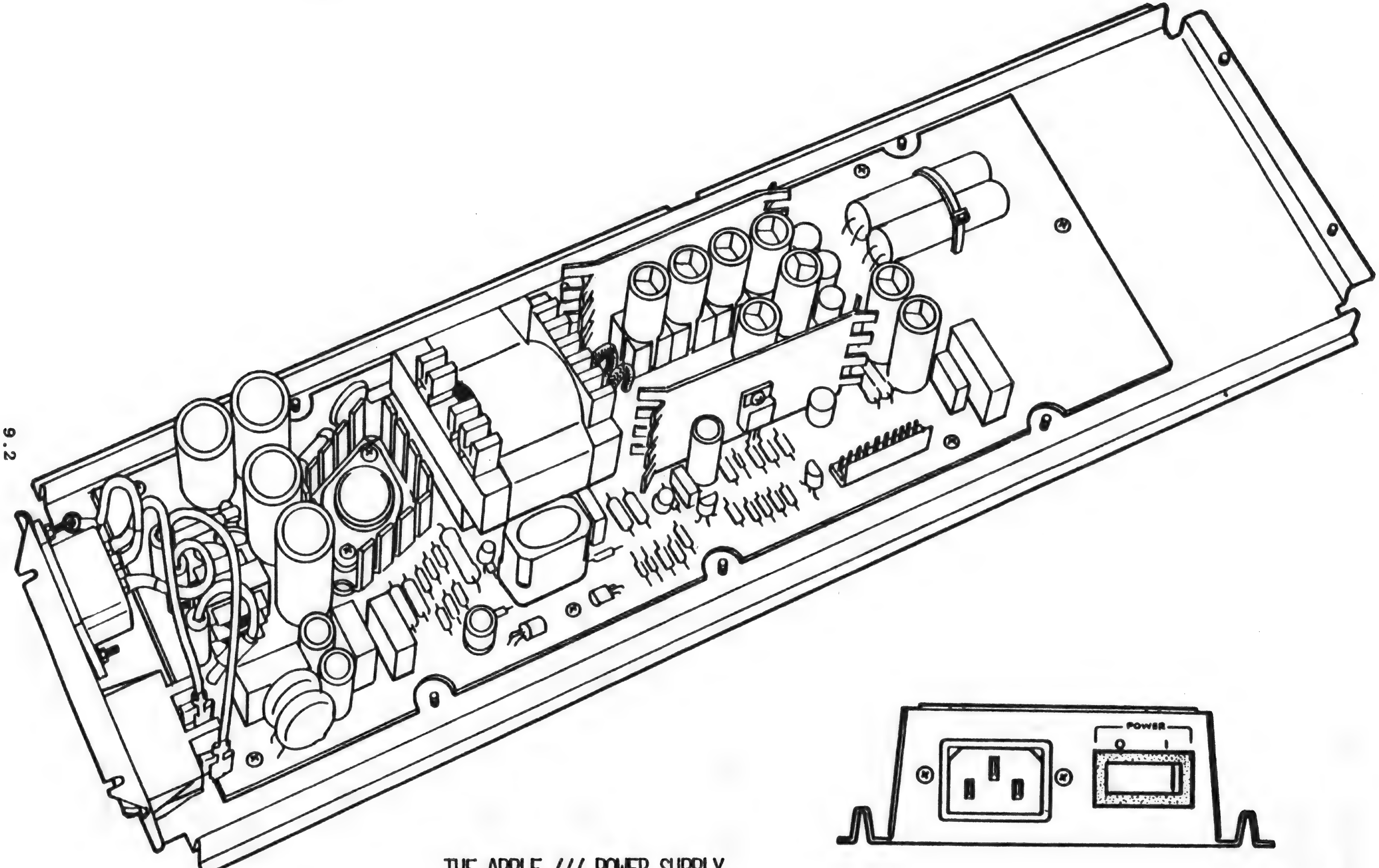
    - Lower power is dissipated because of the on/off role of the regulator. The switching transistors dissipate very little power when either saturated (on) or cutoff (off). With less wasted power, the switching power supply runs at cooler temperatures and costs less to operate.

2. Size and Weight

    - Because components such as capacitors, transformers, and inductors operate at high switching rates they can be smaller and weigh less than those that operate at power line frequencies.

3. Operating Conditions

    - The switching power supply can operate under low AC conditions and can sustain (holdup) its output if input power is momen-



THE APPLE /// POWER SUPPLY
PARTS LAYOUT

tarily lost. This is because the AC input is rectified and the filter capacitors charge to peak voltages on the AC line.

Disadvantages

1. Transient Recovery Time

   - The dynamic loading regulation is slower than that of the series regulated supply. The recovery is limited mostly by the inductance of the output filter network.

2. EMI (Electro-Magnetic Interference)

   - This is a natural byproduct of this type of power supply. This EMI can be conducted to the load (resulting in higher output ripple and noise), and it can be conducted back into the AC line. (Now you know where that stuff on TV came from).

   - Apple designed this power supply with filter networks and shielding to greatly reduce EMI.

HOW IT WORKS!

Regulation is accomplished by a switching transistor Q2 operating under control of a feedback network. The feedback network, consisting of a voltage comparitor and blocking oscillator, controls the duty cycle of the oscillator.

The energy is transferred from the primary to the secondary of the transformer and delivered to the output rectifier/filter. Here the waveform is rectified and averaged to provide a DC output level that is proportional to the duty cycle of the waveform.

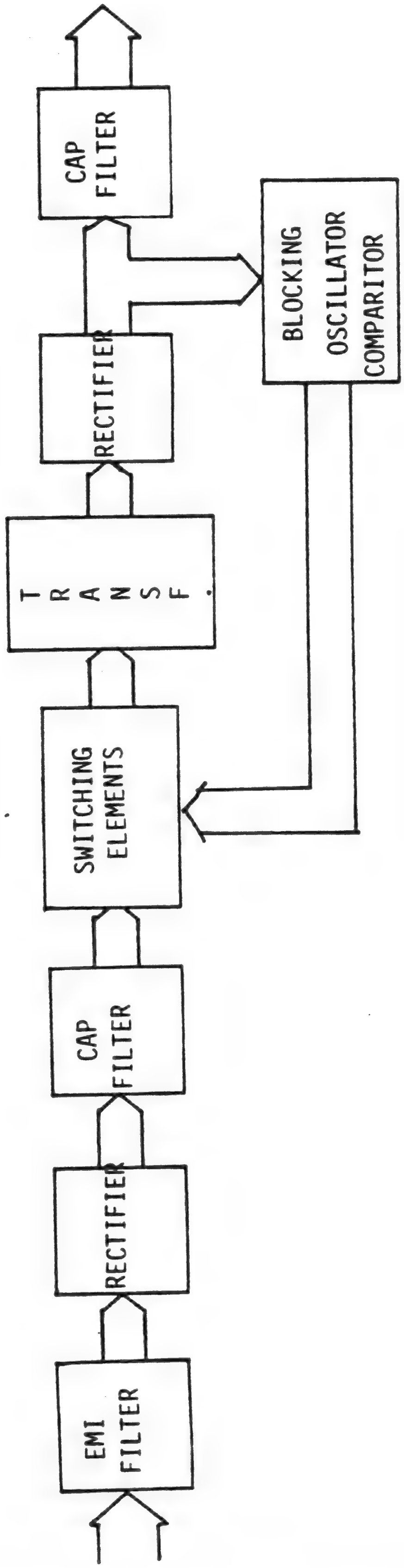
Referring to the block diagram, Figure x.x below, note that:

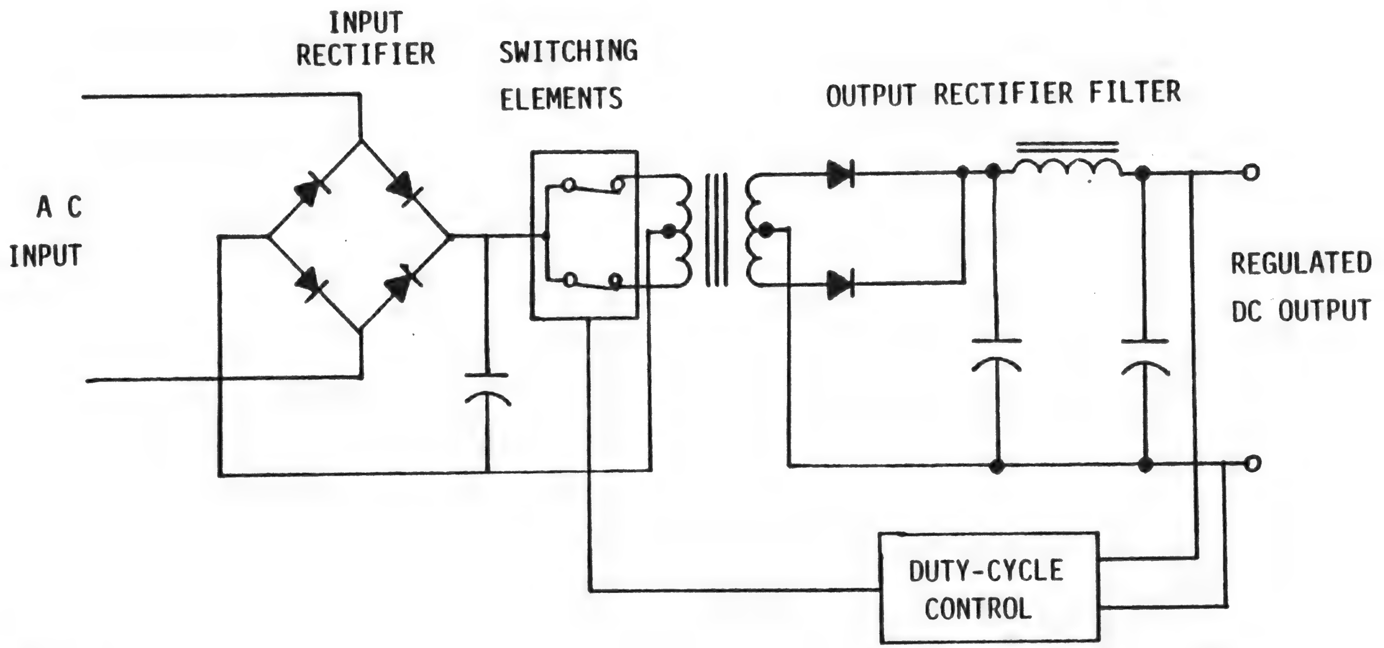
- The AC is passed through an EMI filter and then rectified to provide approximately 300 VDC across the capacitive input filters (C6, C7, C8, C9 of the schematic diagram). This voltage is applied to the primary of the transformer (T2) by the switching elements (turning on power transister Q2). A linear current ramp is developed by the primary inductance of the transformer.

- When the switching elements are turned off, the energy stored in the transformer is transferred to a second set of rectifiers through a capacitive filter network to provide filtering of the output.

- The +5 volt output of the final rectifier network is compared to a reference voltage, and the error is fed back to a blocking oscillator.

- The blocking oscillator basically changes the frequency depending on the output voltage. This in turn changes the repetition rate of the switching elements, which changes the energy transfer through the transformer and voltage output. This is how regulation is accom-


EMI FILTER
RECTIFIER
CAP FILTER
SWITCHING ELEMENTS
TRANSF.
RECTIFIER
CAP FILTER
BLOCKING OSCILLATOR COMPARITOR


INPUT RECTIFIER
SWITCHING ELEMENTS
OUTPUT RECTIFIER FILTER
A C INPUT
REGULATED DC OUTPUT
DUTY-CYCLE CONTROL

plished.

- If the output voltage should change in such a way that the blocking oscillator goes into saturation, the output is essentially cut off.

## DETAILED HARDWARE DESCRIPTION [Refer to Schematic]

A THERMISTOR, R1, is used to limit AC input surge current by its negative temperature coefficient of resistance. When cold, during turn on, R1 has a high resistance; after it heats up, R1 has a low resistance.

VDR1 is a varistor and is used as a transient suppressor. It keeps voltage spikes that result from power supply switching from affecting the performance of the power supply. It basically provides AC line surge current protection at turn on.

THE AC LINE SELECTABLE JUMPER, when connected to 220V position, causes the power supply to act as a conventional full wave rectifier. For 120V AC inputs the input circuitry becomes a voltage doubler.

THE EMI FILTER made up of T1, L1, L2, and C1, helps prevent high frequency RFI spikes from being conducted to the load or back into the AC line.

DB1 is a diode rectifier bridge.

THE SWITCHING ELEMENT consists of the circuitry associated with Q2 and Q1. You may recall that the linear current ramp, developed in the primary of the transformer when Q2 is turned on, is transferred to the secondary when Q2 is turned off.

The turn on of Q2 is accomplished by R2 for starting, and thereafter by the feedback winding in T2 driven by R4 and C10. This winding initiates turn on during the ringdown following the flyback.

If a sufficient voltage is developed across R9, Q1 will be forward bias. This would occur if by chance one of the output voltages were shorted. In that case, the oscillator would stop and shut off all the outputs, pause for 1/2 second, and attempt to restart.

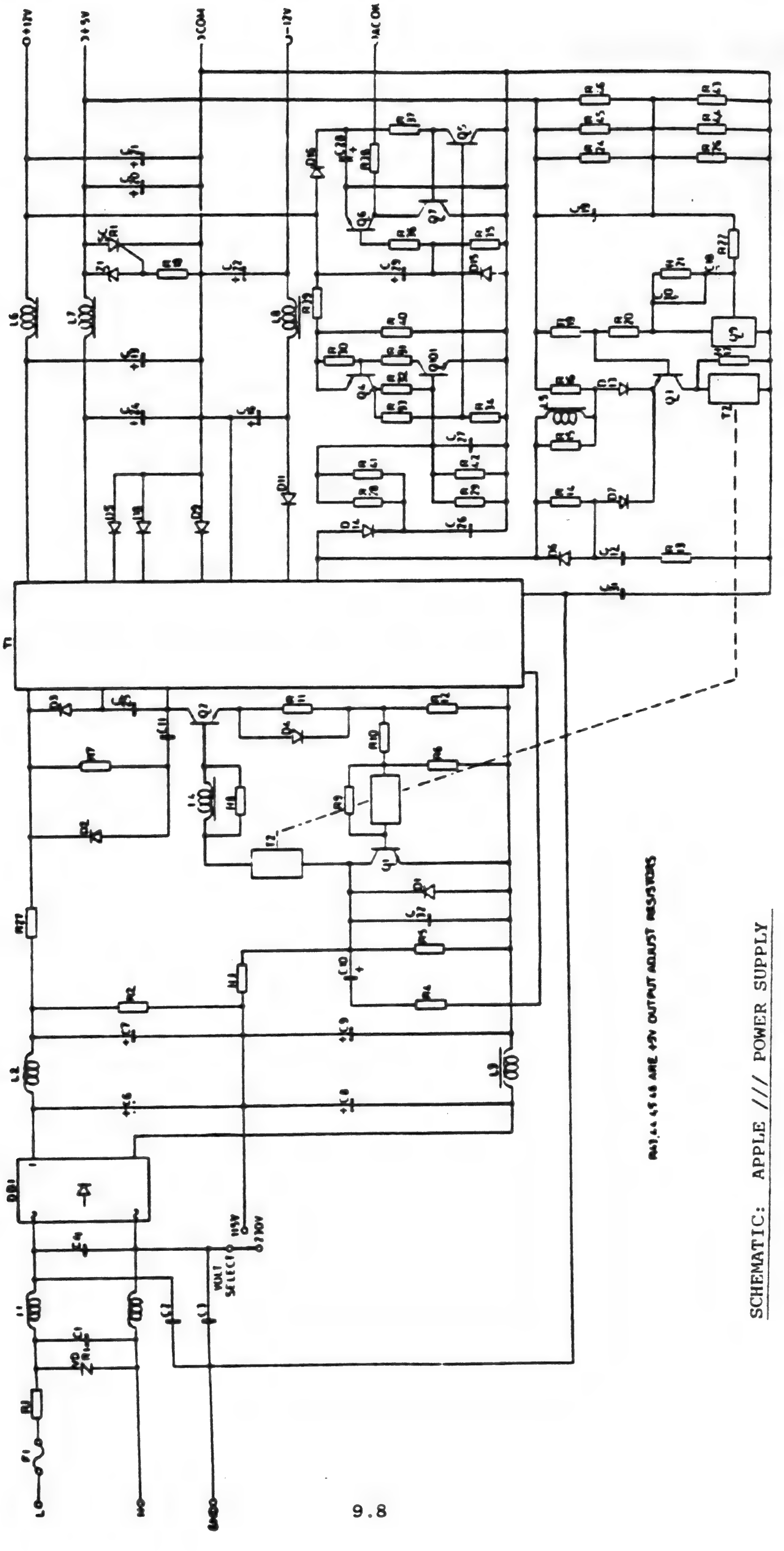
THE OUTPUT RECTIFIER DIODES, D7 through D12, provide rectification, but also protect internal components against reverse currents that could be injected into supply by an active load.

IC1 helps accomplish regulation by comparing the output voltage against its own internal reference and delivering a voltage level to the base of Q3.

The emitter of Q3 is driven by a positive going ramp created by the inductive resistance associated with R14 while Q2 is on. When this voltage is sufficient to forward bias the emitter-base junction of Q3, conduction of Q2 is terminated.

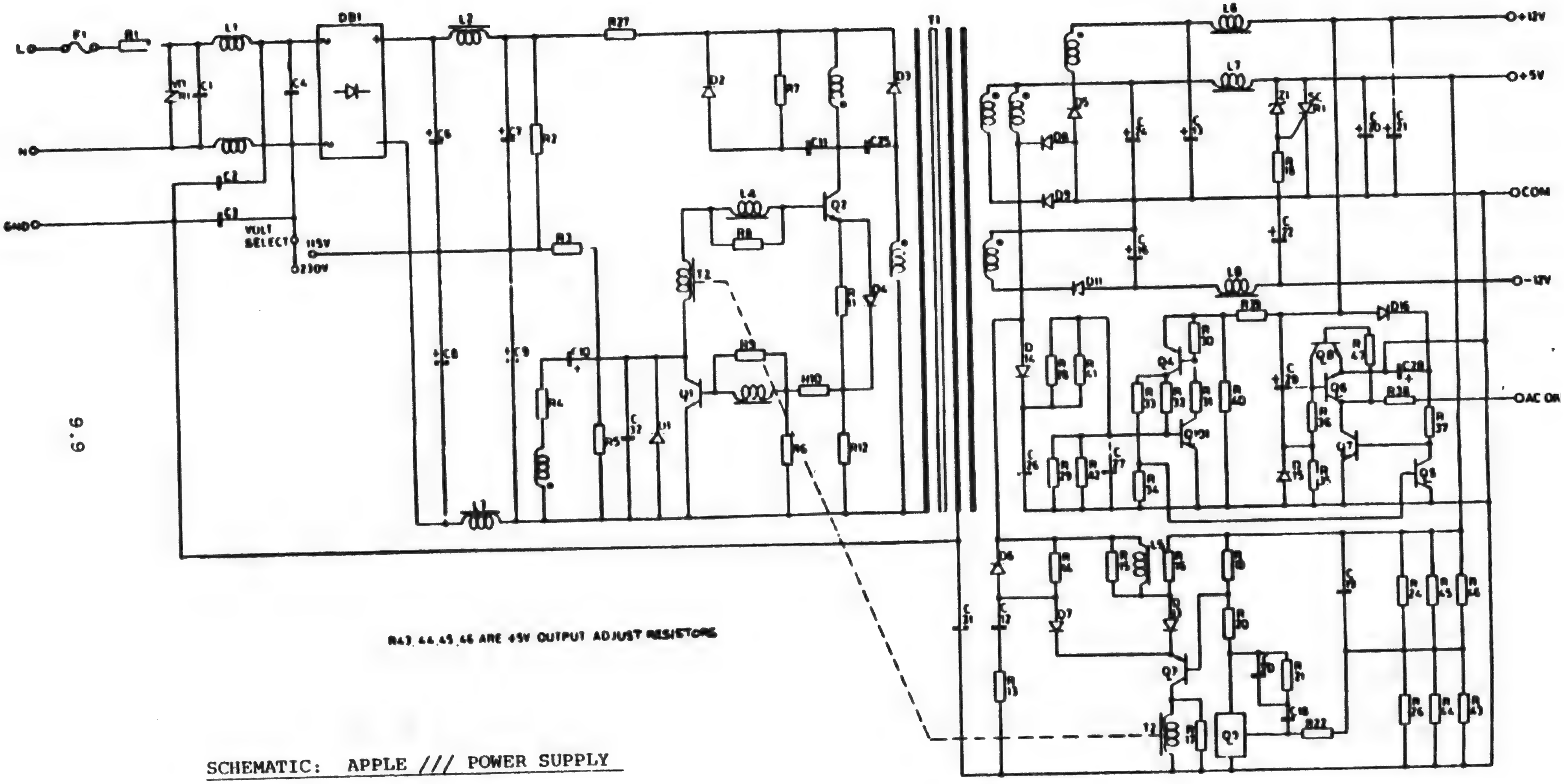
You can now see that the operating frequency varies with the line and load.

OVERVOLTAGE PROTECTION is accomplished by sensing the +12V level via the resistor voltage divider of R17 and R18, referenced to the zener voltage on Z1. When the +12V output rises above tolerance, Q4 is turned on, which in turn triggers SCR1. SCR1 then clamps the +12V to ground, causing the power supply to fold back.


+12V
+5V
COM
-12V
AC OK
T1
DB1
115V
230V
VOLT SELECT
LO
HI
GND

R43,44,45,46 ARE +5V OUTPUT ADJUST RESISTORS

SCHEMATIC: APPLE /// POWER SUPPLY


L
N
GND
F1
R1
VR1
C1
L1
C2
C3
C4
DB1
VOLT SELECT
115V
230V
L2
L3
C6
C7
C8
C9
R2
R3
R4
R5
C10
C32
Z1
R27
D2
D3
D4
R7
C11
C25
L4
R8
Q2
Q1
T2
R9
R10
R11
R12
R6
T1
L6
L7
L8
D5
D8
D9
D11
C14
C15
C16
C20
C21
C22
R18
R19
R30
Z1
ZR1
+12V
+5V
COM
-12V
AC OK
D14
D15
D16
Q3
Q4
Q5
Q6
Q7
Q8
Q9
C26
C27
C28
C29
R29
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R47
D13
L5
D6
D7
C17
C18
C19
C31
R13
R14
R15
R16
R17
R20
R21
R22
C30
R43
R44
R45
R46
R24
R25
R26

R43,44,45,46 ARE +5V OUTPUT ADJUST RESISTORS

SCHEMATIC: APPLE /// POWER SUPPLY

# APPLE III POWER SUPPLY

| REF | DESCRIPTION | QTY | PART NUMBER |
|---|---|---|---|
| | AC Input Socket | | 149-00200020 |
| | Connector Housing 1 CCT | 1 | 138-00000170 |
| | Crimp Terminal | 1 | 403-02200510 |
| | Double Side Tape Width=3x4mm | 20 | 027-01400010 |
| | Faston Tab | 1 | 403-02200700 |
| | Heatsink | 1 | 398-00200060 |
| | Insulator 298. 45X88.9MM | 1 | 183-00101410 |
| | Nut M3 P=0.5 MS/NP | 2 | 394-00400011 |
| | On/Off Switch | 1 | 278-01100010 |
| | Pan | 1 | 403-01101810 |
| | PHL Pan M.C Screw M#x12 P=0.5 BS/NP | 2 | 391-20204141 |
| | PHL Pan M.C Screw M3X8 P=0.5 BS/NP | 3 | 391-20204061 |
| | PHL Pan M/C Screw M3X8 P=0.5 BS/NP | 1 | 391-20204021 |
| | PVC Coating CU Wire 100MM UL1015 | 1 | 356-12200571 |
| | PVC Coating CU Wire 80MM UL1015 | 1 | 357-11800545 |
| | PVC Coating CU Wire 95MM UL1015 | 1 | 356-12200566 |
| | Rectifier RG3B | 3 | 226-10700011 |
| | Resistor, 68K +-5% 1/4W, Carbon Film | 2 | 240-68306022 |
| | Resistor, 82K +-5% 1/4W, Carbon Film | 2 | 240-82306022 |
| | SCR C122u | 1 | 227-13000010 |
| | Solder Bar | 1 | 366-00130010 |
| | Solder Bar 60/40 | 0 | 366-00130010 |
| | Spring Washer M3 BS/NP | 10 | 392-00800031 |
| | Standoff M3 | 8 | 393-00200100 |
| BR1 | Bridge Rectifier KBP10 | | 226-30500010 |
| C01 | Cap, 0.22uf, 250VAC, Metallized Paper | 1 | 068-22400010 |
| C02 | Cap 0.1uf, 250VAC, Metallized Paper | 1 | 068-10400010 |
| C03 | Cap, 4700pf, 400 VAC, Ceramic | 2 | 055-47220001 |
| C04 | Cap, 4700pf, 400 VAC, Ceramic | 2 | 055-47220001 |
| C05 | Cap, 0.1uf, 400 V, Polyester | 1 | 058-10400100 |
| C06 | Cap, 100uf, 250V, Electrolytic | 4 | 057-101201170 |
| C07 | Cap, 100uf, 250 V, Electrolytic | 4 | 057-101201170 |
| C08 | Cap, 100uf, 250v, Electrolytic | | 057-10120170 |
| C09 | Cap, 100uf, 250V, Electrolytic | 4 | 057-101201170 |
| C10 | Cap, 100uf, 250V, Electrolytic | 1 | 057-22120080 |
| C11 | Cap, 0.001uf, 3KV, Ceramic | | 055-10261328 |
| C12 | Cap, 22uf, 100V, Polyester | 2 | 058-22400120 |
| C13 | Cap, 1000uf, 10V, Electrolytic | 6 | 057-10220020 |
| C14 | Cap, 1000uf, 10V, Electrolytic | 6 | 057-10220020 |
| C15 | Cap, 1000uf, 10V, Electrolytic | 6 | 057-10220020 |
| C16 | Cap, 1000uf, 10V, Electrolytic | 6 | 057-10220020 |
| C17 | Cap, 330uf, 16V, Electrolytic | | 057-33120080 |
| C18 | Cap, 22ouf, 10V, Electrolytic | 1 | 057-22120060 |
| C19 | Cap, 0.22uf, 100V, Polyester | 1 | 058-22300080 |
| C20 | Cap, 1000uf, 10V, Electrolytic | | 057-10220020 |
| C21 | Cap, 0.22uf, 100V, Polyester | | 058-22400120 |
| C22 | Cap, 1000uf, 10V, Electrolytic | | 057-10220020 |
| C23 | Cap, 330uf, 16V, Electrolytic | 3 | 057-33120080 |
| C24 | Cap, 680uf, 16V, Electrolytic | 1 | 057-68120010 |
| C25 | Cap, 330uf, 16V, Electrolytic | 3 | 057-33120080 |
| C26 | Cap, 0.1/1KV, Ceramic | 1 | 055-10360925 |
| D01 | Diode, Rectifier, RGP10A | 1 | 226-10400050 |
| D02 | Diode, Rectifier, RGP10M | 2 | 226-10400100 |
| D03 | Diode, Recitifier, RGP10M | 2 | 226-10400100 |

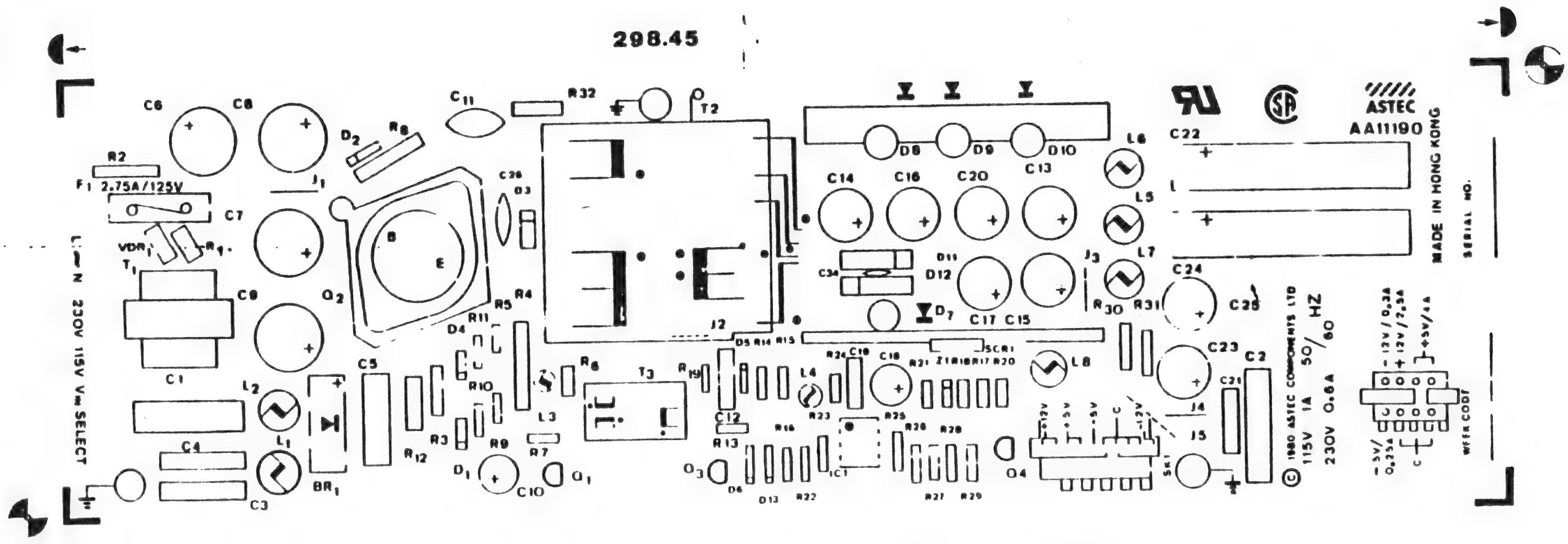
## APPLE III POWER SUPPLY

| REF | DESCRIPTION | QTY | PART NUMBER |
|---|---|---|---|
| D04 | Diode, Rectifier, 1N4001GP | 1 | 226-10400080 |
| D05 | Diode, Silicon, 1N5282 | 3 | 212-10700200 |
| D06 | Diode, Silicon, 1N5282 | 3 | 212-10700200 |
| D07 | Diode, Rectifier/Scr Assembly |  | 853-00700010 |
| D08 | Diode, Rectifier assembly |  | 853-00200140 |
| D09 | Diode, Rectifier Assembly |  | 853-00200140 |
| D10 | Rectifier Assembly |  | 853-00200140 |
| D11 | Schottky Diode S3SC3M |  | 212-31100030 |
| D12 | Rectifier RG3B | 1 | 226-10700010 |
| D13 | Diode, Silicon, 1N5282 | 3 | 212-10700200 |
| F1 | Fuse 2.75A 125V | 1 | 084-00200040 |
| IC1 | Integrated Circuit, Regulator, TL431CP | 1 | 211-10800070 |
| J1 | Jumper Wire | 4 | 358-80810011 |
| J2 | Jumper Wire | 4 | 358-80810011 |
| J3 | Jumper Wire | 4 | 358-80810011 |
| J4 | Jumper Wire | 40 | 358-80800001 |
| L1 | Choke | 2 | 852-20100350 |
| L2 | Choke | 2 | 852-20100350 |
| L3 | Base Choke | 1 | 328-00100030 |
| L4 | Choke 1.5mH | 1 | 328-00100010 |
| L5 | Choke Coil Assembly | 1 | 852-20100010 |
| L6 | Choke Coil | 1 | 852-10100370 |
| L7 | Choke Coil | 1 | 328-00100060 |
| L8 | Choke Coil | 1 | 328-00100060 |
| Q1 | Transistor SD467 | 1 | 209-11700463 |
| Q2 | Transistor 2SC1358 | 1 | 209-10200010 |
| Q3 | Transistor SB561 | 2 | 210-11700353 |
| Q4 | Transistor SB561 | 2 | 210-11700353 |
| R01 | Thermistor, 4R @25 C +-10% 6R @ 25 C +-20% | 1 | 258-40970015 |
| R02 | Resistor, 150K +-5% 1/2W | 2 | 240-15406033 |
| R03 | Resistor, 150K +-5% 1/2W |  | 240-15406033 |
| R04 | Resistor, +-5% 47R 2W, Metal Oxide | 1 | 248-47006063 |
| R05 | Resistor, +-5% 1/4W 1.2K | 1 | 240-12206022 |
| R06 | Resistor, 5.6R +-5% 1/4W | 1 | 240-56906022 |
| R07 | Resistor, +-5% 56R 1/4W, Carbon film |  | 240-56006022 |
| R08 | Resistor, +5% 120R 2W | 1 | 248-12106063 |
| R09 | Resistor, +-5% 1/4W 15R | 2 | 240-15006022 |
| R10 | Resistor, +-5% 1/4W 10R, Carbon Film | 1 | 240-10006022 |
| R12 | Resistor, 0.47R, Metal Film | 1 | 247-04786054 |
| R13 | Resistor, -5% 1/4W 39R, Carbon Film | 1 | 240-39006022 |
| R14 | Resistor, +-5% 270R 1/4W | 2 | 240-27106033 |
| R15 | Resistor, +-5% 270R 1/4W, Carbon Film |  | 240-27106033 |
| R16 | Resistor, 8.2 +-5% 1/4W, Carbon Film | 1 | 240-82906022 |
| R17 | Resistor, +-5% 680R 1/4W | 1 | 240-68106022 |
| R18 | Resistor, +-5% 1.8K, Carbon Film | 1 | 240-18206022 |
|  | Resistor, +-5% 2.2K, Carbon Film | 1 | 240-22206022 |
|  | Resistor, +-5% 2.7K 1/4W, Carbon Film | 1 | 240-27206022 |
| R19 | Resistor, +-5% 560R 1/4W, Carbon Film | 1 | 240-56106022 |
| R20 | Resistor, 22R 1/4W +-5%, Carbon film | 1 | 240-22006022 |
| R21 | Resistor, 100R +-5% 1/4W, Carbon Film | 1 | 240-10106022 |
| R22 | Resistor, 56R +-5% 1/4W, Carbon Film | 3 | 240-56006022 |
| R23 | Resistor, 56R +-5% 1/4W, Carbon film |  | 240-56006022 |
| R243 | Resistor, 12K +-5% 1/4W, Carbon Film | 1 | ✓ 240-12306022 |
| R25 | Resistor, +-5% 1/4W 470R, Carbon Film |  | 240-47106022 |

# APPLE III POWER SUPPLY

| REF | DESCRIPTION | QTY | PART NUMBER |
|---|---|---|---|
| R26 | Resistor, +-2% 2.7K 1/4W, Metal Film | 2 | 247-2701502 |
| R27 | Resistor, +-2% 2.7K 1/4W, Metal Film |  | 247-27015022 |
| R28 | Resistor, 100K +-5% 1/4W, Carbon Film | 2 | 240-10406022 |
| R29 | Resistor, 100K +-2% 1/4W, Carbon Film |  | 240-10406022 |
| R30 | Resistor, -5% 56R 1W, Matal Oxide Filmm | 1 | 248-56006052 |
| R31 | Resistor, +-5% 220R 1W, Metal Oxide Film | 1 | 248-22106052 |
| R32 | Resistor, 1R !w, Metal film | 1 | 247-10086054 |
| T1 | Common Mode Choke Assembly | 1 | 852-20200010 |
| T2 | Power Transformer assembly | 1 | 852-10200760 |
| T3 | Control Transformer Assembly | 1 | 852-10200680 |
| VDRL | Varistor 260VAC | 1 | 256-26100014 |
| Z1 | Zener Diode 9.6 to 10.V @ 1mA | 1 | 222-98085002 |

# THE APPLE /// POWER SUPPLY
## COMPONENT LAYOUT


298.45
C6
C8
C11
R32
T2
D2
R8
R2
F1 2.75A/125V
C7
J1
C26
D3
VDR1
R1
T1
B
E
Q2
C9
C1
L2
L1
C4
C3
BR1
C5
R12
R3
R11
R5
R4
D4
R10
R9
D1
C10
Q1
R7
L3
R6
T3
R19
J2
C12
R13
Q3
D6
D13
D5 R14 R15
R16
R22
R24 C19
L4
R23
IC1
C18
R21 Z1 R18 R17 R20
SCR1
R25
R26
R28
R27
R29
D8
D9
D10
C14
C16
C20
C13
C34
D11
D12
D7
C17 C15
L8
Q4
SK1
L6
L5
L7
J3
R30
R31
C22
C24
C25
C23
J4
J5
C21
C2
ASTEC
AA11190
MADE IN HONG KONG
SERIAL NO.
© 1980 ASTEC COMPONENTS LTD
115V 1A 50/60 HZ
230V 0.6A
- 12V / 0.2A
+ 12V / 2.5A
+5V/4A
- 5V/ 0.25A
C
WEEK CODE
L N 230V 115V Vin SELECT
2 JAN 1980

# APPLE II EMULATION RESTRICTIONS

- NO LANGUAGE CARD
- NO ROM CARD
- PADDLES ARE DIFFERENT
- ENTER WITH SOFTWARE BUT ONLY RESET WILL EXIT

## THE COLOR VIDEO CONNECTOR

| Pin | Name | Description |
|---|---|---|
| 1 | SG | Shield Ground. |
| 2 | XRGB4 | One of four GRB outputs. This (and pins 5, 9, and 10) is a TTL output with instantaneous color information. A linear weighted sum of these four signals will form a true 16-color RGB video signal |
| 3 | SYNCH | Composite synchronization signal with negative-going tips. |
| 4 | PDI | Not used. |
| 5 | XRGB1 | See pin 2. |
| 6 | GND | Power and signal ground. |
| 7 | -5V | -5 volt power supply. A device may draw up to 200 ma through this pin. |
| 8 | +12V | +12 volt power supply. A device may draw up to 500 ma through this pin. |
| 9 | XRGB2 | See pin 2. |
| 10 | XRGB8 | See pin 2. |
| 11 | BWVID | Black and white composite video. This is an NTSC composite video signal with negative-going synch tips, 1 volt peak-to peak into a 75 ohm load. Color information is encoded as a linear grey scale. |
| 12 | NTSC | Color composite video. This is an NTSC-compatible video signal with negative-going sych tips, 1 volt peak-to-peak into a 75 ohm load. |
| 13 | GND | Power and signal ground. |
| 14 | -12V | -12 volt power supply. A device may draw up to 200 ma through this pin. |
| 15 | +5V | +5 volt supply. A device may draw up to 1 amp through this pin. |

This connector supplies 7 different video signals and 4 power supply voltages. Through this connector you can hook up the Apple to any NTSC color or black and white video monitor. With an additional circuit you can hook up the Apple to a studio-quality RGB color monitor.

All power supply current ratings assume that no peripheral cards are installed in the system. If there are cards in the system, be sure to account for the current drawn by those cards.

## THE HIGH-RESOLUTION GRAPHICS (HI-RES) MODE

The Apple ][ emulation mode high resolution graphics are identical to the Apple ][ except some combinations of colors on the right edge of the screen will cause the left edge pixels to blink. This is normal though distracting.

## THE SPEAKER

The speaker function is identical to the Apple ][ with the following additional features.

A reference to location 49216 (or the equivalent addresses -16336 or hexadecimal $C040) will cause a 0.1 second 1 KHz tone to be produced which is similar to the sound the AUTOSTART monitor makes when the BELL character is sent to the screen. The advantage to this is 0.1 seconds of cpu time is returned to the user since only 1 microsecond is required to start the BELL sound.

The AUDIO connector at the back of the Apple /// provides the same signal as the speaker. When you insert a miniature phone-tip plug into this jack, the Apple's internal speaker is silenced; if there is an amplifier or other device properly connected to the plug, then that device will receive all audio signals generated by the Apple. The signal is a 0.5 volt peak-to-peak audio signal on its tip and signal ground on its ring.

## THE CASSETTE INTERFACE

The cassette interface is completely eliminated on the Apple ///. References to the cassette output port at 49184 (or the equivalent -16352 of hexadecimal $C020) will cause pin 39 of the I/O slots to go low for a microsecond. This is for use by Apple /// native mode peripherals to deselect to $C800 ROM address space.

Reading the cassette input port at 49248 or the equivalents -16288 or hexadecimal $C060 will read joystick switch 0 into bit 7.

## Table 10: Input / Output Special Locations

| Function | Address: | | | Read/Write |
|---|---|---|---|---|
| | Decimal | | Hex | |
| Speaker | 49200 | -16336 | $C030 | R/W |
| Beep | 49216 | -16320 | $C040 | R/W |
| Deselect $C800 for Apple /// periperals (pin 39 in slots) | 49184 | -16352 | $C020 | R/W |
| Joystick switch 0 | 49248 | -16288 | $C060 | R(bit 7) |
| Joystick switch 1 | 49249 | -16287 | $C061 | R(bit 7) |
| Joystick switch 2 | 49250 | -16286 | $C062 | R(bit 7) |
| Joystick switch 3 | 49251 | -16285 | $C063 | R(bit 7) |
| $\overline{\text{A/D Select 0}}$ | 49240 | -16296 | $C058 | R/W |
| A/D select 0 | 49241 | -16295 | $C059 | R/W |
| $\overline{\text{A/D Select 1}}$ | 49246 | -16290 | $C05E | R/W |
| A/D Select 1 | 49247 | -16289 | $C05F | R/W |
| $\overline{\text{A/D Select 2}}$ | 49242 | -16294 | $C05A | R/W |
| A/D Select 2 | 49243 | -16293 | $C05B | R/W |
| A/D Ramp charge | 49244 | -16292 | $C05C | R/W |
| A/D Start timeout | 49245 | -16291 | $C05D | R/W |
| $\overline{\text{A/D Timeout}}$ | 49254 | -16282 | $C066 | R(bit 7) |
| Clock millisecond counter ($NO) | 49264 | -16272 | $C070 | R(bits 7-4) |

## Table 9: A/D Selection

| A/D 2 | A/D 1 | A/D 0 | Input |
|---|---|---|---|
| 0 | 0 | 0 | Ground |
| 0 | 0 | 1 | Joystick, Port B, X axis |
| 0 | 1 | 0 | Joystick, Port B, Y axis |
| 0 | 1 | 1 | Joystick, Port A, X axis |
| 1 | 0 | 0 | Joystick, Port A, Y axis |
| 1 | 0 | 1 | Clock Battery |
| 1 | 1 | 0 | No connection |
| 1 | 1 | 1 | Reference Voltage |

## ANALOG INPUTS

The system has two joystick ports with provisions for two A/D inputs each. Joystick Port A reads A/D inputs 0 and 2 while Port B reads inputs 1 and 3 as defined in BASIC and the monitor subroutine PREAD.

To read the A/D inputs, the software must select the desired input and charge the ramp capacitor for at least 500 microseconds. Then the ramp is started and the time measured until the A/D timeout goes low. The discharge time is proportional to the input voltage.

## STROBE OUTPUT

The strobe output ($C040) has been replaced by a 0.1 second 1 KHz tone from the speaker.

## AUTOSTART ROM / MONITOR ROM

The Apple ][ emulation only comes with a modified version of the Autostart ROM. This is in write protected RAM which is loaded when the Apple ][ emulation disk is booted.

## THE SYSTEM MONITOR

### SAVING A RANGE OF MEMORY ON THE TAPE

Since there is no cassette port on the Apple /// the W (for WRITE) command has no effect. The code in the Emulation mode Autostart Monitor contains an RTS instruction followed by NOP instructions, followed by BRK instructions. This fills the space occupied by the WRITE subroutine (locations $FECD-$FEF4).

### READING A RANGE FROM TAPE

Again, since there is no cassette port the R (READ) command has no effect. The READ subroutine contains an RTS followed by NOP instructions, followed by BRK instructions (locations $FEFD-$FF2C).

### SOME USEFUL MONITOR SUBROUTINES

#### $FB1E PREAD READ A JOYSTICK AXIS

PREAD will return a number which represents the position of a joystick axis. You should pass the number of the joystick axis (0 to 3) in the X register. If this number is greater than 3, port A, Y axis is read. PREAD returns a number from $00 to $FF in the Y register. The accumulator is scrambled.

| Joystick | Reference # |
|---|---|
| Port A, X axis | 0 |
| Port B, X axis | 1 |
| Port A, Y axis | 2 |
| Port B, Y axis | 3 |

## Page Three Monitor Locations

| Address:<br>Decimal | Hex | Use: |
|---|---|---|
| 1008<br>1009 | $3F0<br>$3F1 | Holds the address of the subroutine which handles machine language "BRK" requests (normally $FA59). |
| 1010<br>1011 | $3F2<br>$3F3 | Soft Entry Vector. These two locations contain the address of the reentry point for whatever language is in use. Normally contains $E003. |
| 1012 | $3F4 | Power-up byte. Normally contains $45. |
| 1013<br>1014<br>1015 | $3F5<br>$3F6<br>$3F7 | Holds a "JuMP" instruction to the subroutine which handles Applesoft ][ "&" commands. Normally $4C $58 $FF. |
| 1016<br>1017<br>1018 | $3F8<br>$3F9<br>$3FA | Holds a "JuMP" instruction to the subroutine which handles "USER" (CONTROL Y) commands. |

## Built-In I/O Locatons

| | $0 | $1 | $2 | $3 | $4 | $5 | $6 | $7 |
|---|---|---|---|---|---|---|---|---|
| $C000 | Keyboard Port A Input | | | | | | | |
| $C008 | Keyboard Port B Input | | | | | | | |
| $C010 | Clear Keyboard Strobe | | | | | | | |
| $C020 | Deselect all expansion I/O space (pin 39) for Apple /// cards | | | | | | | |
| $C030 | Speaker Toggle (1us) pulse | | | | | | | |
| $C040 | Speaker Beep (1 KHz for 0.1 second) | | | | | | | |
| $C050 | gr | tx | nomix | mix | pri | sec | lores | hires |
| $C058 | $\overline{\text{A/D 0}}$ | A/D 0 | $\overline{\text{A/D 2}}$ | A/D 2 | A/D CHG | A/D ST | $\overline{\text{A/D 1}}$ | A/D 1 |
| $C060 | SW0 | SW 1 | SW 2 | SW 3 | $\overline{\text{IRQ 2}}$ | $\overline{\text{IRQ 1}}$ | $\overline{\text{A/D TM}}$ | MUX1 |
| $C070 | Clock millisecond output ($NO) | | | | | | | |

$C090-$C09F Slot 1 Device Select (pin 41) goes low during C1M

$C0A0-$C0AF Slot 2 Device Select (pin 41) goes low during C1M

$C0B0-$C0BF Slot 3 Device Select (pin 41) goes low during C1M

$C0C0-$C0CF Slot 4 Device Select (pin 41) goes low during C1M

$C0E0 $\overline{\text{Disk Stepper Motor Phase A}}$

$C0E1 Disk Stepper Motor Phase A

$C0E2 $\overline{\text{Disk Stepper Motor Phase B}}$

$C0E3 Disk Stepper Motor Phase B

$C0E4 $\overline{\text{Disk Stepper Motor Phase C}}$

$C0E5 Disk Stepper Motor Phase C

$C0E6 $\overline{\text{Disk Stepper Motor Phase D}}$

$C0E7 Disk Stepper Motor Phase D

| | |
|---|---|
| $C0E8 | Disk motor off |
| $C0E9 | Disk motor on |
| $C0EA | Select Drive 1 (Built-in) |
| $C0EB | Select Drive 2 (First external) |
| $C0EC | Q6L |
| $C0ED | Q6H |
| $C0EE | Q7L |
| $C0EF | Q7H |
| $C0F0 | ACIA Receive/Transmit Data register |
| $C0F1 | ACIA Status register |
| $C0F2 | ACIA Command register |
| $C0F3 | ACIA Control register |
| $C100-$C1FF | Slot 1 I/O Select (Pin 1) goes low during C1M low |
| $C200-$C2FF | Slot 2 I/O Select (Pin 1) goes low during C1M low |
| $C300-$C3FF | Slot 3 I/O Select (Pin 1) goes low during C1M low |
| $C400-$C4FF | Slot 4 I/O Select (Pin 1) goes low during C1M low |

## PERIPHERAL BOARD I/O

The Apple /// implements only slots 1 through 4. Slot 6 is always a disk interface card and slots 5 and 7 emulate either a SERIAL or COMMUNICATIONS card. Slot 0 scratchpad RAM exists but no provision is made to put a LANGUAGE card or FIRMWARE card into the system. Thus the RAM is limited to 48K with a 12K ROM chosen at Boot time.

## PERIPHERAL CARD I/O SPACE

Slot 6 device I/O space $C0E0-$C0EF contains the hardware for the disk interface. Slot 7 device I/O space $C0F0-$C0F3 contains the addresses for the onboard ACIA.

## PERIPHERAL CARD ROM SPACE

Slot 5 and slot 7 contain code which is functionally equivalent to the COMMUNICATIONS or SERIAL card for the Apple ][. They differ in that they use the built-in ACIA. For a more complete explanation see "SERIAL AND COMMUNICATONS CARD EMULATION ".

Slot 6 contains a copy of the Apple ][ 16 sector Boot PROM.

## ROM MEMORY

The Applesoft, Integer Basic, and Autostart Monitor "ROMS" are actually write protected RAMs in the Apple ///. When the Emulation mode disk is booted it loads RAM memory with an image of each set of ROMs. Whichever language is selected when the Apple ][ disk is booted is loaded into the address space ($D000-$FFFF) and write protected.

## RAM MEMORY

In Emulation mode there is always 48K of RAM. It is addressed $0000 to $BFFF. There is no provision for a slot 0 Language or Firmware card.

## "USER 1" JUMPER

There is no "User 1" jumper in the Apple ///.

## THE GAME I/O CONNECTOR

There is no 16 pin Game I/O connector in the Apple ///. However there are two 9 pin "D" - joystick connectors.

## THE JOYSTICK PORTS

The Apple /// has to joystick ports (A and B). The A port will NOT operate a silentype printer in Emulation mode. The physical pinout is:

```
5   4   3   2   1
  9   8   7   6
```

## PORT A PINOUT

| Pin | Name | Description |
|---|---|---|
| 1 | SGND | Shield ground. |
| 2 | +5V | +5 volt power supply. |
| 3 | GND | Power and Signal Ground. |
| 4 | X0 | Horizontal analog input, PDL (0) in BASIC. |
| 5 | SW1 | Joystick switch 1, orange button. |
| 6 | +12V | +12 volt power supply. |
| 7 | GND | Power and signal Ground. |
| 8 | Y0 | Vertical analog input, PDL (2) in BASIC. |
| 9 | SW3 | Joystick switch 3. |

## PORT B PINOUT

| Pin | Nmae | Description |
|---|---|---|
| 1 | SGND | Shield Ground. |
| 2 | +5V | +5 volt power supply. |
| 3 | GND | Power and Signal ground. |
| 4 | X1 | Horizontal analog input, PDL (1) in BASIC. |
| 5 | SW2 | Joystick switch 2, orange button. |
| 6 | +12V | +12 volt power supply. |
| 7 | GND | Power and signal ground. |
| 8 | Y1 | Vertical analog input, PDL (3) in BASIC. |
| 9 | SW0 | Joystick switch zero. |

## THE KEYBOARD

The keyboard is different in design but the locations of the Keyboard Data Input and the Clear Keyboard Strobe are the same. For more information see "THE KEYBOARD" in chapter 1.

## CASSETTE INTERFACE JACKS

There are no cassette interface jacks in the Apple ///.

## POWER CONNECTOR

The power connector is different but is not user accessible.

## SPEAKER

The speaker is identical to the Apple ][.

## PERIPHERAL CONNECTORS

The Apple ][ emulation redefines a few of the pins on the connector and adds several new ones.

The most significant difference is that interrupts will not be sent to the 6502 from the slots. In fact the IRQ (pin 30) is an input to the cpu so the card can't even determine if an interrupt is occuring. Thus Emulation mode runs without interrupts, period.

The RES (pin 31) is an output to the card and goes low when the RESET key is pressed on the keyboard. However the microprocessor is actually performing an NMI not a RESET.

## Peripheral Connector Pinout

| | | | |
|---|---|---|---|
| GND | 26 | 25 | +5V |
| DMAOK | 27 | 24 | NOT USED |
| $\overline{\text{DMAI}}$ | 28 | 23 | NOT USED |
| $\overline{\text{IONMI}}$ | 29 | 22 | $\overline{\text{TSADE}}$ (Open collector) |
| $\overline{\text{IRQ}}$ | 30 | 21 | RDY (Open collector) |
| $\overline{\text{IORES}}$ | 31 | 20 | $\overline{\text{I/O STROBE}}$ |
| $\overline{\text{INH}}$ | 32 | 19 | PH0 |
| -12V | 33 | 18 | $\text{R}/\overline{\text{W}}$ |
| -5V | 34 | 17 | A15 |
| SYNC | 35 | 16 | A14 |
| C7M | 36 | 15 | A13 |
| Q3 | 37 | 14 | A12 |
| $\overline{\text{C1M}}$ | 38 | 13 | A11 |
| $\overline{\text{IOCLR}}$ | 39 | 12 | A10 |
| C1M | 40 | 11 | A9 |
| $\overline{\text{DEV SEL}}$ | 41 | 10 | A8 |
| D7 | 42 | 9 | A7 |
| D6 | 43 | 8 | A6 |
| D5 | 44 | 7 | A5 |
| D4 | 45 | 6 | A4 |
| D3 | 46 | 5 | A3 |
| D2 | 47 | 4 | A2 |
| D1 | 48 | 3 | A1 |
| D0 | 49 | 2 | A0 |
| +12V | 50 | 1 | $\overline{\text{I/O SELECT}}$ |

# Peripheral Connector Signal Description

| Pin: | Name: | Description: |
|---|---|---|
| 1 | $\overline{\text{I/O SELECT}}$ | This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PHO (nominally 500ns) and will drive 12 LSTTL loads. |
| 2-17 | A0-A15 | The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PHO. These lines will each drive 8 LSTTL loads. |
| 18 | R/$\overline{\text{W}}$ | Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads. |
| 19 | PHO | A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs. |
| 20 | $\overline{\text{I/O STROBE}}$ | This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads. |
| 21 | RDY | The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output. |
| 22 | $\overline{\text{TSADB}}$ | A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output. |
| 23 |  | Not used in an Apple ///. |
| 24 |  | Not used in an Apple ///. |
| 25 | +5V | Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board). |
| 26 | GND | System circuit ground. 0 volt line from power supply. Do not use for shield ground. |
| 27 | DMAOK | Acknowledge signal to the peripheral following |

| | | |
|---|---|---|
| | | its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed. |
| 28 | $\overline{\text{DMAI}}$ | Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output. |
| 29 | $\overline{\text{IONMI}}$ | Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output. |
| 30 | $\overline{\text{IRQ}}$ | This line is ignored in Apple ][ emulation mode. It should be driven by a TTL output. |
| 31 | $\overline{\text{IORES}}$ | Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads. |
| 32 | $\overline{\text{INH}}$ | Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output. |
| 33 | -12V | Negative 12 volt supply, 200mA total for all peripheral boards together. |
| 34 | -5V | Negative 5 volt supply, 200mA total for all periperal boards together. |
| 35 | SYNC | The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads. |
| 36 | C7M | Seven MHz high frequency clock. Will drive 10 LSTTL loads. |
| 37 | Q3 | A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs. |
| 38 | $\overline{\text{C1M}}$ | Complement of C1M clock. This will drive 12 LSTTL loads. |
| 39 | $\overline{\text{IOCLR}}$ | Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple ][ peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads. |
| 40 | $\overline{\text{C1M}}$ | Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads. |
| 41 | $\overline{\text{DEVICE SELECT}}$ | This line becomes acive (low) on each peripheral |

| | | |
|---|---|---|
| | | connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads. |
| 42-49 | D7-D0 | The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{\text{C1M}}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{\text{C1M}}$. These lines will drive 8 LSTTL inputs. |
| 50 | +12V | Positive 12 volt supply, 300mA total for all peripheral boards together. |

# ROM LISTINGS

## APPLE ][ EMULATION MODE AUTOSTART ROM LISTING

The following is a listing of addresses which changed content in the Autostart ROM to eliminate cassette I/O, read joysticks, and redirect the NMI vector to the RESET code.

```
;       THE ACIA IS CAPABLE OF GENERATING INTERRUPTS IN EMULATION MODE.
;        IF IT DOES THE INTERRUPT RECEIVER SETS THE PROCESSOR INTERRUPT
;        INHIBIT BIT TO PREVENT THE SERVICING OF THIS INTERRUPT


FA49: 4C 10 FF            JMP IHBIRQS       ;JMP TO CODE TO INHIBIT INTERRUPTS

FF10: 68                  PLA               ;GET PROCESSOR STATUS BYTE
FF11: 09 04               ORA #$04          ;SET INTERRUPT INHIBIT BIT
FF13: 48                  PHA               ;PUT STATUS BYTE BACK ON STACK
FF14: A5 45               LDA $45           ;RESTORE ACCUMULATOR
FF16: 40                  RTI               ;RETURN WITH INTERRUPTS INHIBITTED


;       THE RESET KEY IN EMULATION MODE GENERATES AN NMI (NONMASKABLE
;        INTERRUPT).  THEREFORE THE NMI VECTOR IS SET TO POINT AT THE
;        RESET CODE WHICH ALSO MAKES SURE THE DISK MOTOR STOPS


FFFA: 62 FA               DFB     RESET     ;POINT NMI VECTOR TO RESET CODE

FA62: D8         RESET    CLD               ;BINARY ARITHMATIC PLEASE
FA63: AD EE C0            LDA     $C0EE     ;SET DISK READ
FA66: AD EC C0            LDA     $C0EC
FA69: AD E8 C0            LDA     $C0E8     ;TURN OFF DISK
FA6C: 20 84 FE            JSR     SETNORM
FA6F: 20 2F FB            JSR     INIT
FA72: 20 93 FE            JSR     SETVID
FA75: 20 89 FE            JSR     SETKBD
FA78: EA                  NOP
FA79: EA                  NOP
FA7A  EA                  NOP


;       THE CASSETTE READ ROUTINE SIMPLY RETURNS TO USER CALLS
```

```
FEFD: 60          READ    RTS       ;NO CASSETTE PORT - RETURN TO USER

FEFE-FF0A: EA             NOP       ;FILL CODE WITH NOPS
FF0B: 22
FF0C-FF0F: 00             BRK       ;STOP USER FROM JUMPING INTO MIDDLE OF CODE
FF17-FF2C: 00             BRK


;        THE CASSETTE WRITE ROUTINE SIMPLY RETURNS TO USER CALLS


FECD: 60                  RTS       ;NO CASSETTE PORT - RETURN TO USER

FECE-FEF2: EA             NOP       ;FILL CODE WITH NOPS
FEF3-FEF5: 00             BRK       ;STOP USER JUMPING INTO CODE


;        READ JOYSTICK AXIS.  THIS IS THE SAME ENTRY ADDRESS OF PREAD
;         WHICH READS THE GAME PADDLES IN THE APPLE ][
;
;        X REGISTER CONTAINS JOYSTICK AXIS AND Y RETURNS $00-$FF OF JOYSTICK
;
;                X REGISTER      JOYSTICK AXIS
;
;                    0           PORT A, X AXIS
;                    1           PORT B, X AXIS
;                    2           PORT A, Y AXIS
;                    3           PORT B, Y AXIS


FB1E: 8A          PREAD   TXA                 ;SAVE X REGISTER
FB1F: 48                  PHA
FB20: 49 01               EOR #$01            ;REMAP JOYSTICK ADDRESS
FB22: AA                  TAX
FB23: AD 59 C0            LDA $C059           ;SET ANALOG MUX TO PORT B, X AXIS
FB26: AD 5E C0            LDA $C05E
FB29: AD 5A C0            LDA $C05A
FB2C: 4C C9 FC            JMP JOY2

FCC9: E8          JOY2    INX
FCCA: CA                  DEX                 ;SET FLAGS
FCCB: F0 12               BEQ JOY3            ;PORT B, X AXIS?
FCCD: AD 5F C0            LDA $C05F           ;NO
FCD0: CA                  DEX
FCD1: F0 0C               BEQ JOY3            ;PORT A, X AXIS?
FCD3: AD 58 C0            LDA $C058           ;NO
FCD6: CA                  DEX
FCD7: F0 06               BEQ JOY3            ;PORT B, Y AXIS?
FCD9: AD 5E C0            LDA $C05E           ;NO
```

```
FCDC: AD 5B C0          LDA $C05B       ;MUST BE PORT A, Y AXIS
FCDF: AD 5C C0   JOY3   LDA $C05C       ;CHARGE CAPACITOR
FCE2: A9 0F             LDA #$0F        ;WAIT 800US
FCE4: 20 A8 FC          JSR WAIT
FCE7: A0 80             LDY #$80
FCE9: AD 5D C0          LDA $C05D       ;START TIMEOUT
FCEC: A2 48             LDX #$48        ;WAIT 370US
FCEE: CA         JOY4   DEX
FCEF: 10 FD             BPL JOY4
FCF1: E8         JOY5   INX
FCF2: B9 E6 BF          LDA $BFE6,Y     ;FALSE READ
FCF5: 2A                ROL
FCF6: AD 66 C0          LDA $C066       ;BIT 7 IS VOLTAGE CROSSOVER
FCF9: 30 F6             BMI JOY5        ;HAS VOLTAGE CROSSED OVER?
FCFB: 8A                TXA             ;YES
FCFC: 10 04             BPL JOY6        ;WAS COUNT POSITIVE?
FCFE: A9 FF             LDA #$FF        ;NO
FD00: D0 01             BNE JOY7        ;USE $FF
FD02: 2A         JOY6   ROL             ;DOUBLE COUNT
FD03: A8                TAY             ;RETURN COUNT IN Y
FD04: 68                PLA             ;RESTORE X
FD05: AA                TAX
FD06: 60                RTS

FD07-FD0B: 00           BRK             ;FILL SPACE
```

**NOTE:** UNLESS OTHERWISE SPECIFIED

1. ⬭ = 75 Ω

2. ⬭ (UUT) = ALL UNITS UNDER TEST MOLEX PINS TO BE LOCATED TOGETHER.

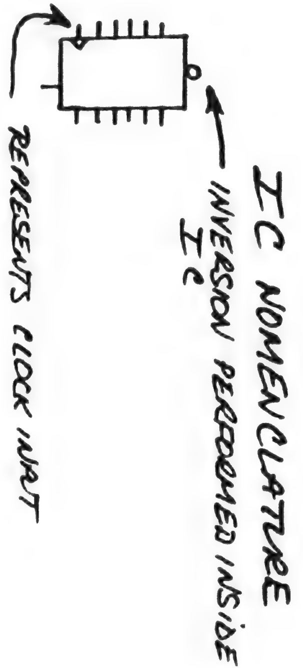
3. ○ = ALL TIMING MOLEX PINS TO BE LOCATED TOGETHER.

4. THIS SCHEMATIC REPRESENTS ASSY 610-0105 AT REV LEVEL: F.

◁ FOR STANDARD SYSTEMS G9 IS 341-0030, FOR EURO SYSTEMS G9 IS 341-0060.

▷ FOR STANDARD SYSTEMS Y1 IS 14.318630 MHZ, FOR EURO SYSTEMS Y1 IS 14.250450 MHZ.

| REV | ZONE | ECO # | REVISION | APPD |
|---|---|---|---|---|
| C2 | | | ENG. RELEASE | |
| C3 | | | PRE-PRODUCTION RELEASE | |
| E | | | PRE-PRODUCTION CHANGES | |
| E | | 504 | ECO RELEASE | |
| F | | 544 | DELETED CAP ARRAY (CP1), AND N13, M13, K13, N3, N10 WAS RC NETWORK. C5 WAS 47pF. Q1 WAS QØ N.C. IS NOW IOSTOPD. J20, 7 WAS COLORKILL. J20, 9 WAS FORCPAGE. DELETED MICROPROCESSER (33) | |
| G | | 773 | H3 WAS LS04; R15 WAS 47 OHM, R16 WAS 75 OHM. ADDED 1K OHM RESISTOR AT K10. | |



SIGNAL SOURCES ARE DESIGNATED BY PAGE AND PAGE LOCATION

5 B4

Page 5 of 10

ALPHA NUMERIC LOCATION

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| ITEM | QTY | PART NUMBER | DESCRIPTION |
|---|---|---|---|

apple computer inc

TITLE: SCHEMATIC APPLE ///
MAIN LOGIC #2

SIZE: C
DRAWING NUMBER: 050-0039-G
SCALE: NONE
SHEET 1 OF 10
MATERIAL: N/A
FINISH: N/A

DRAWING NUMBER 050-0039-G SH 1 OF 10

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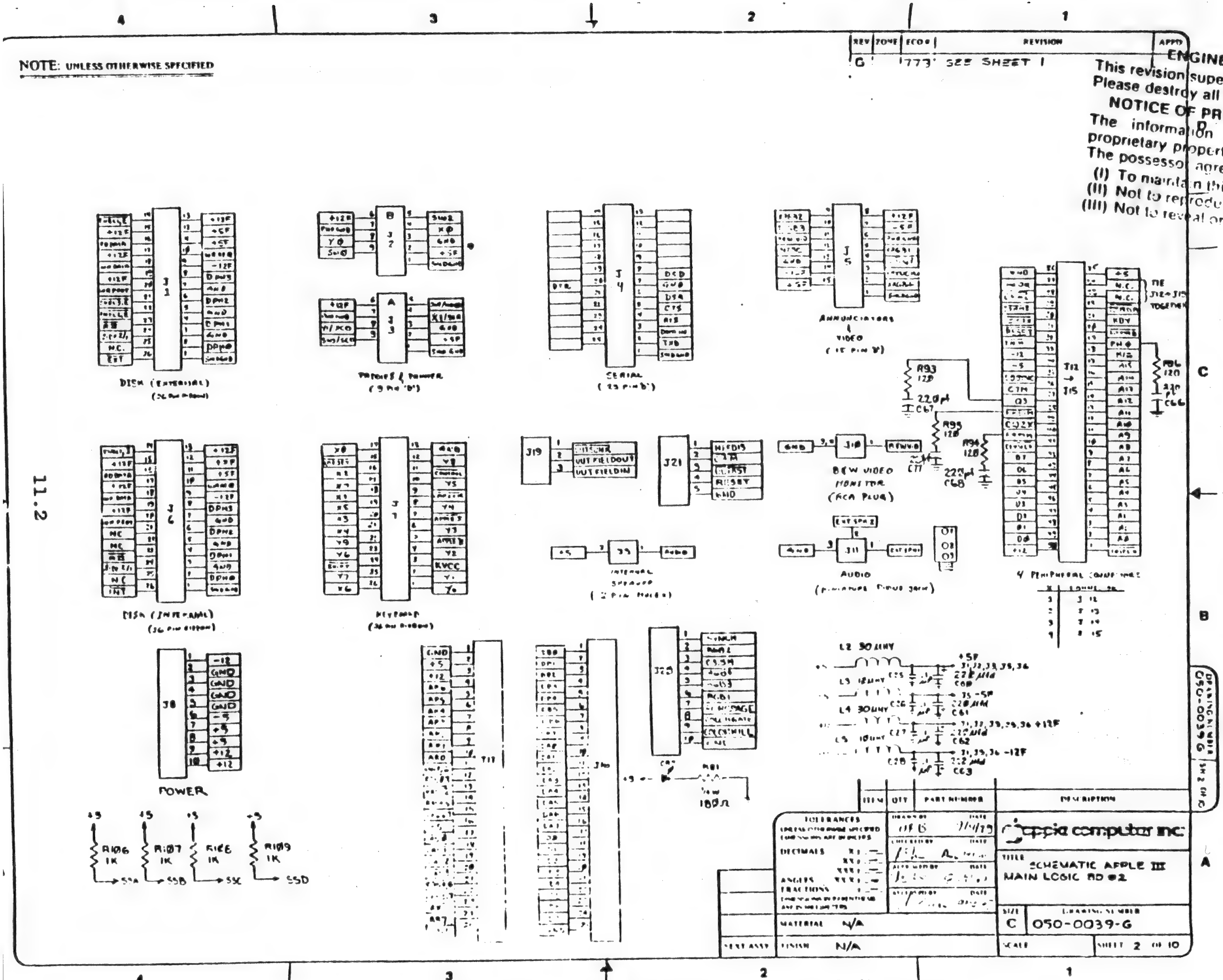
| REV | ZONE | ECO # | REVISION | APPD |
|---|---|---|---|---|
| G |  | 773 | SEE SHEET 1 |  |



J1
DISK (EXTERNAL) (26 PIN RIBBON)
J2
J3
PADDLES & POWER (9 PIN 'D')
J4
SERIAL (25 PIN 'D')
DCD
GND
DSR
CTS
RTS
TXD
DTR
J5
ANNUNCIATORS & VIDEO (15 PIN 'D')
J6
DISK (INTERNAL) (26 PIN RIBBON)
J7
KEYBOARD (26 PIN RIBBON)
J8
POWER
-12
GND
-5
+5
+12
J19
J21
J10
B&W VIDEO MONITOR (RCA PLUG)
J11
AUDIO (MINIATURE PHONE JACK)
J9
INTERNAL SPEAKER (2 PIN MOLEX)
J12 → J15
4 PERIPHERAL CONNECTORS
J16
J17
J25
R93 12Ω
R94 12Ω
R95 12Ω
C67 22.0pf
C68 22.0pf
R96 120
C66
L2 30µHY
L3 10µHY
L4 30µHY
L5 10µHY
C25
C26
C27
C28
C60
C61
C62
C63
+5F
-5F
+12F
-12F
R81 100Ω
R106 1K
R107 1K
R108 1K
R109 1K
SSA
SSB
SSC
SSD
+5
1
2
3
4
A
B
C
D

| ITEM | QTY | PART NUMBER | DESCRIPTION |
|---|---|---|---|

TOLERANCES: UNLESS OTHERWISE SPECIFIED

DECIMALS

ANGLES, FRACTIONS

MATERIAL N/A

FINISH N/A

DRAWN 7/4/79

apple computer inc.

TITLE SCHEMATIC APPLE III MAIN LOGIC BD #2

SIZE C

DRAWING NUMBER 050-0039-G

SHEET 2 OF 10

DRAWING NUMBER 050-0039-G SH 2 OF 10

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| REV | ZONE | ECO # | REVISION | APPD |
|---|---|---|---|---|
|  |  |  | SEE SHT 1 |  |

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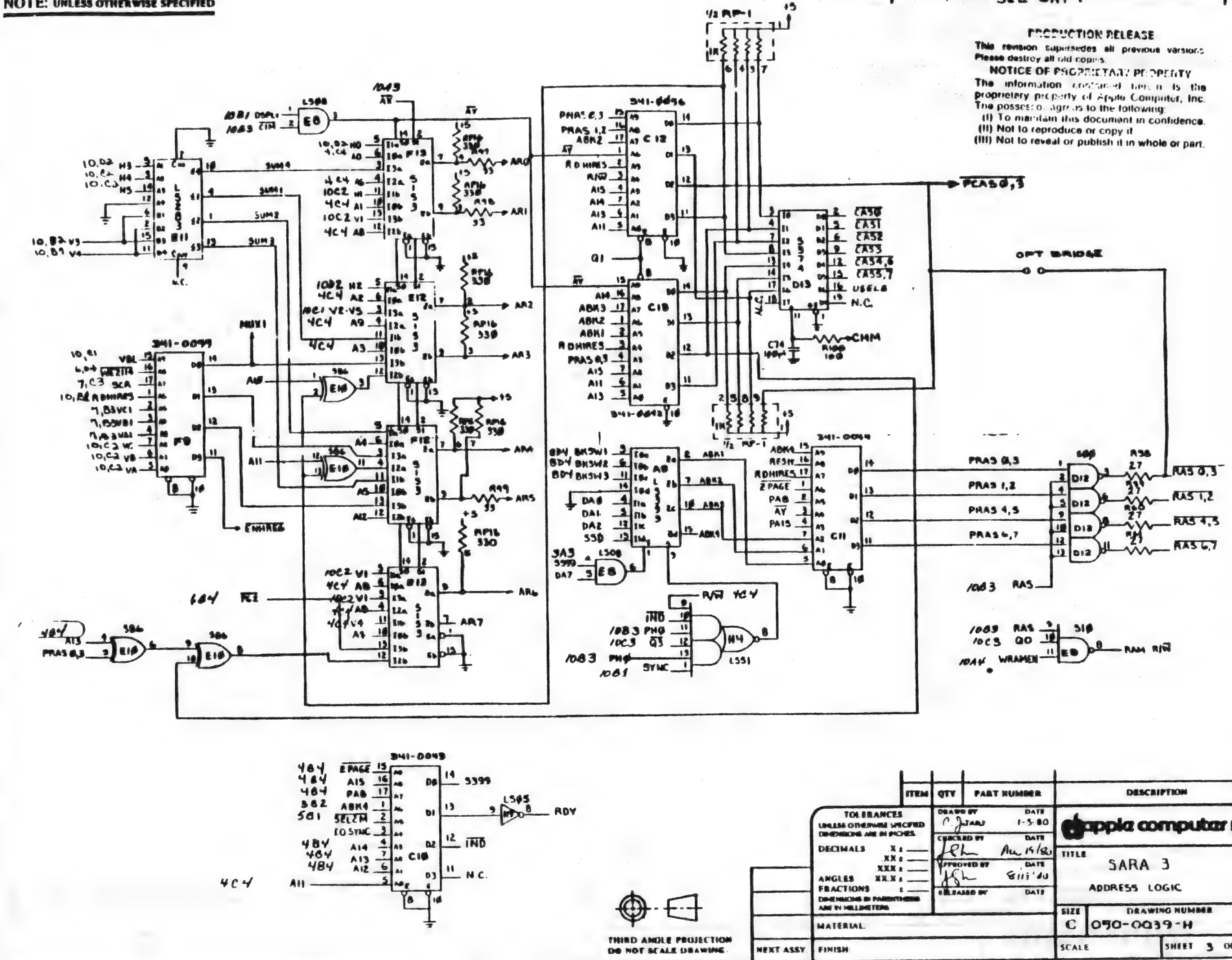
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F9
F13
E12
F12
F11
E10
E8
C12
C10
D13
C11
A8
H4
D12
C18
341-0044
341-0099
341-0096
341-0043
RP-1
SUM0
SUM1
SUM2
SUM3
MUX1
ENHREG
AR0
AR1
AR2
AR3
AR4
AR5
AR6
AR7
PCAS0,3
CAS0
CAS1
CAS2
CAS3
CAS4,6
CAS5,7
USEL8
N.C.
CHM
OPT BRIDGE
PRAS 0,3
PRAS 1,2
PRAS 4,5
PRAS 6,7
RAS 0,3
RAS 1,2
RAS 4,5
RAS 6,7
RAS
RAM R/W
WRAMEN
R/W
INO
PH0
Q3
SYNC
RDY
5399
IND
ZPAGE
A15
PAB
ABK4
SELZM
IO SYNC
A14
A13
A12
A11
4C4
4B4
10B3
1OB3
RDHIRES
R/W
ABK1
ABK2
ABK3
BDY BKSW1
BDY BKSW2
BDY BKSW3
DA0
DA1
DA2
SSD
DA7
3A3
Q1
C74
R100
100
L551
L505
L508
S10
S06
+5

| ITEM | QTY | PART NUMBER | DESCRIPTION |
|---|---|---|---|

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DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES .XXX ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

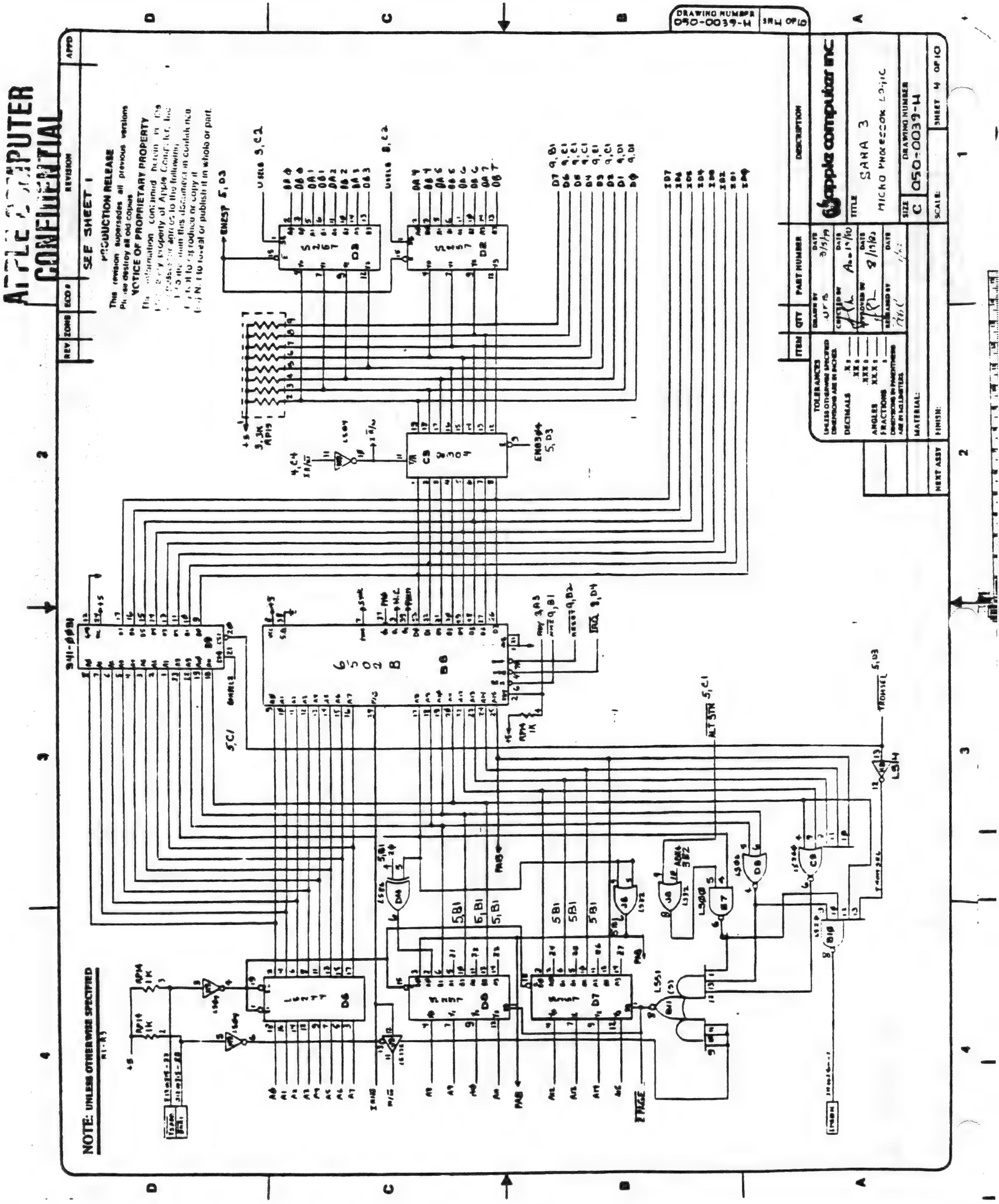
DRAWN BY C. J... DATE 1-5-80
CHECKED BY DATE Au 15/80
APPROVED BY DATE 8/11/80
RELEASED BY DATE

MATERIAL
NEXT ASSY.
FINISH:

apple computer inc
TITLE SARA 3
ADDRESS LOGIC
SIZE C
DRAWING NUMBER 090-0039-H
SCALE
SHEET 3 OF 10

DRAWING NUMBER 090-0039-H SH 3 OF 10

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING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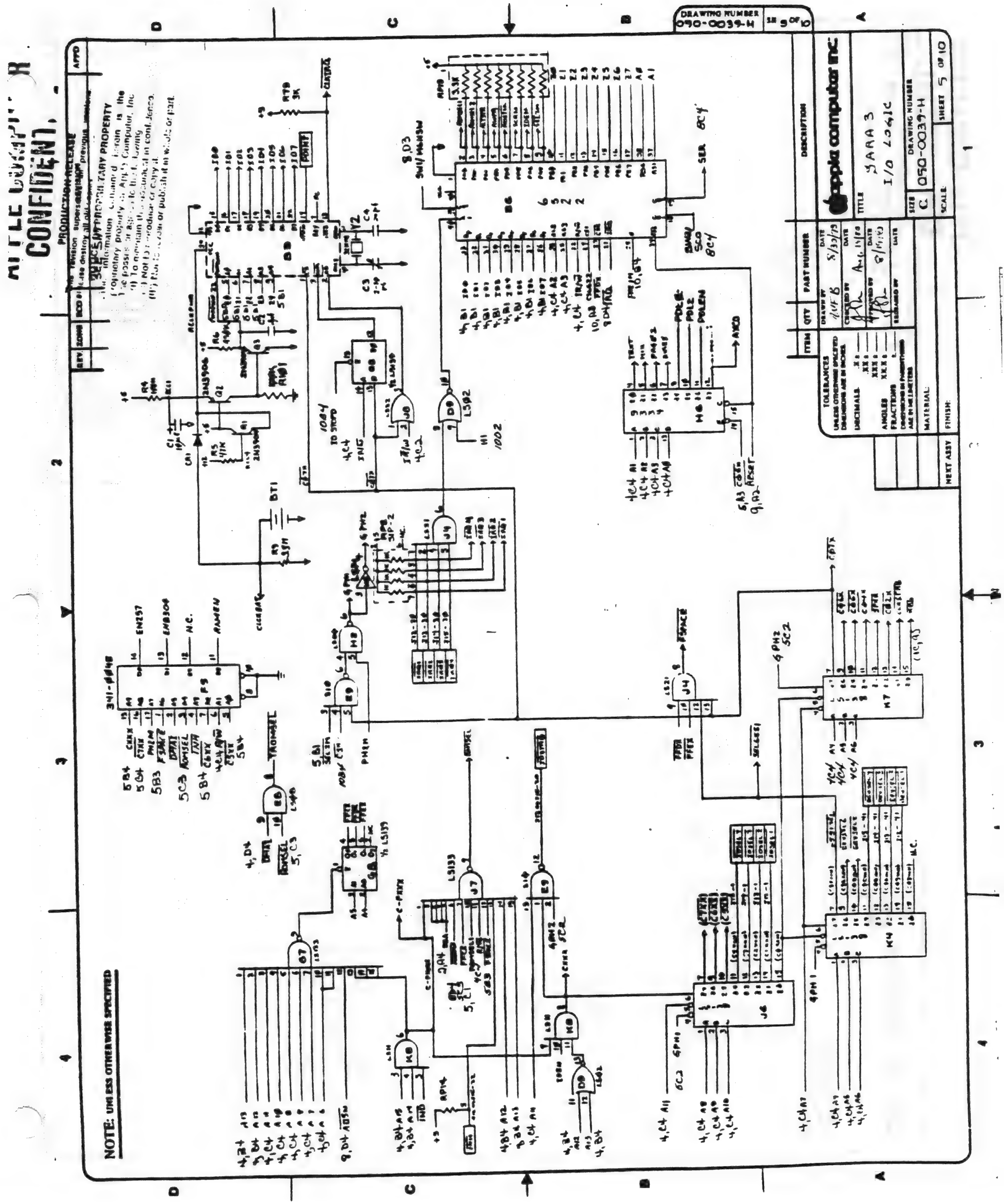
SHEET 4 OF 10
apple computer inc
SARA 3
MICRO PROCESSOR LOGIC
050-0039-H
6502 B
D8
NOTE: UNLESS OTHERWISE SPECIFIED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SH 5 OF 10
apple computer inc
TITLE SARA 3 I/O LOGIC
SIZE C
DRAWING NUMBER 050-0039-H
SHEET 5 OF 10
SCALE
DRAWN BY
CHECKED BY
APPROVED BY
RELEASED BY
DATE 8/30/79
TOLERANCES
DECIMALS
ANGLES
FRACTIONS
MATERIAL
FINISH
NEXT ASSY
ITEM
QTY
PART NUMBER
DESCRIPTION
B6 6522
B8
M6
M7
K4
J6
J7
E9
G7
F8
2N3906
BT1
Y2
NOTE: UNLESS OTHERWISE SPECIFIED

11.5

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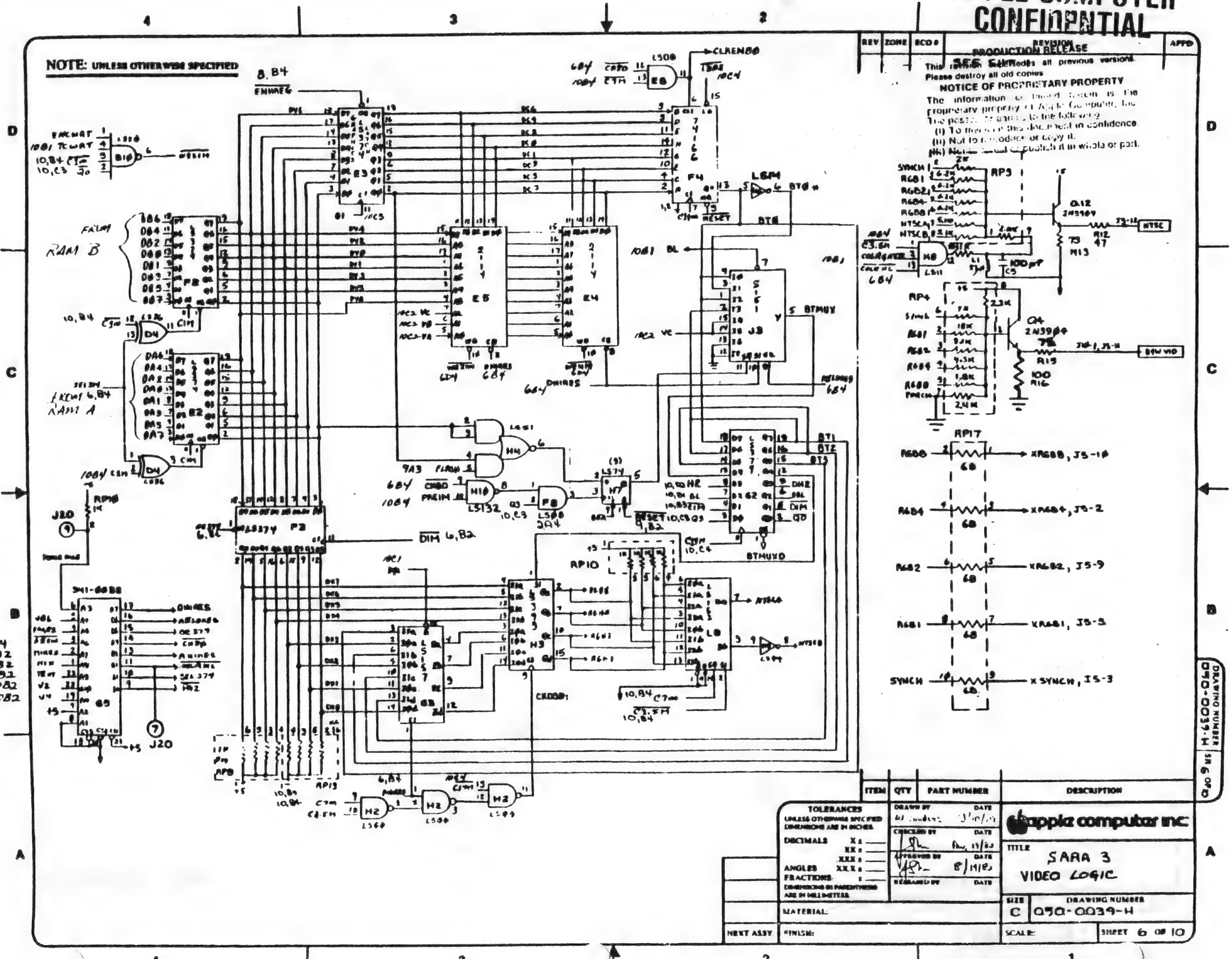
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ENHREG
E3
F4
E5
E4
F2
E2
D4
B10
RAM B
FROM
FROM 6,B4
RAM A
J20
RP18
341-0088
G5
DHIRES
ALTCHAR
CSR374
XHIRES
SEL374
H2
LS374
P3
DIM 6,B2
H4
H10
LS132
F8
LS00
H7
LS74
J3
BTMUX
BTMUXD
G2
H3
CKDDB1
L8
RP10
RP13
RP8
NTSCA
NTSCB
LS04
E8
L5B4
BT0
CLKENB0
10B1 BL
10C2 VC
RP3
RP4
RP17
Q12 2N3904
Q4 2N3904
R12 47
R13 75
R15 75
R16 100
C5 100pF
NTSC
B/W VID
SYNCH
RGB0
RGB1
RGB2
RGB4
XRGB8, J5-10
XRGB4, J5-2
XRGB2, J5-9
XRGB1, J5-5
XSYNCH, J5-3
68
A B C D
1 2 3 4

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FINISH:
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ITEM | QTY | PART NUMBER | DESCRIPTION

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APPROVED BY | DATE 8/19/82
RELEASED BY | DATE

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TITLE
SARA 3
VIDEO LOGIC

SIZE C
DRAWING NUMBER 090-0039-H
SCALE:
SHEET 6 OF 10

DRAWING NUMBER 090-0039-H SH 6 OF 10

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|---|---|---|---|---|
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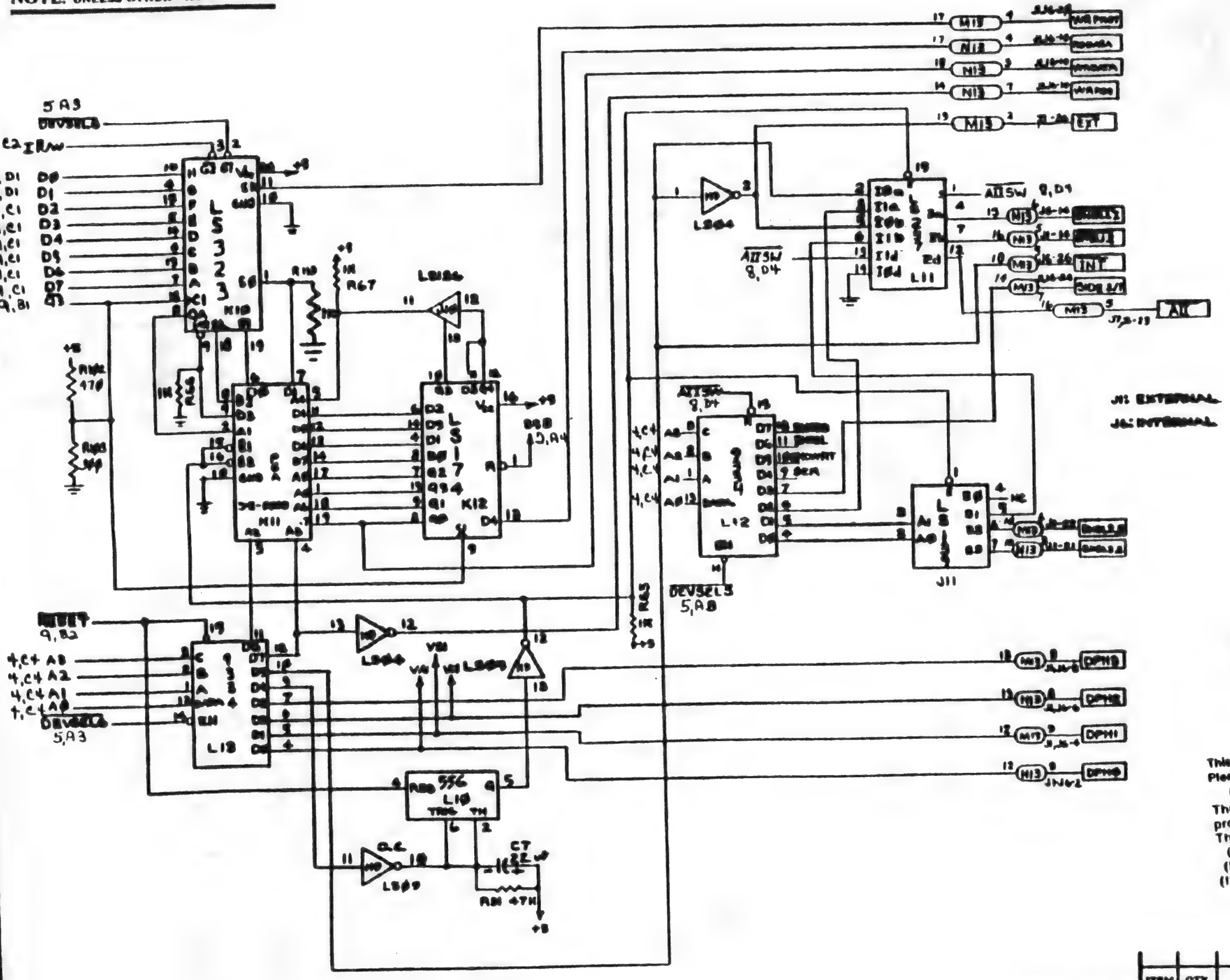

5A3
DEVSEL6
4,C2 IR/W
9,D1 D0
9,D1 D1
9,C1 D2
9,C1 D3
9,C1 D4
9,C1 D5
9,C1 D6
9,C1 D7
9,B1 Q3
LS323
K10
R10
R67 1K
LS126
LS194
K12
DS8
13,A4
M11
RN2 470
RN3 1K
RESET
9,B2
4,C4 A3
4,C4 A2
4,C4 A1
4,C4 A0
DEVSEL6
5,A3
L13
LS04
LS05
556
L10
LS09
CT 22uF
RN 47K
R43 1K
DEVSEL3
5,A8
A11SW
8,D4
L12
J11
L11
A11SW 9,D1
LS04
M13
WR PROT
RDDATA
WRDATA
WREQ
EXT
INT
SIDE 2/1
AII
DPH3
DPH2
DPH1
DPH0
J1: EXTERNAL
J2: INTERNAL

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DRAWING NUMBER 050-0039-H SH 7 OF 10

| ITEM | QTY | PART NUMBER | DESCRIPTION |
|---|---|---|---|

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ANGLES ±
FRACTIONS ±
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DRAWN BY Terry Lurie DATE 1-8-79
CHECKED BY JBL DATE A... 11/80
APPROVED BY JBL DATE 2/15/81
RELEASED BY DATE

apple computer inc

TITLE SARA 3
DISK CONDITIONER
Logic

SIZE C DRAWING NUMBER 050-0039-H
SCALE REV D SHEET 7 OF 10

MATERIAL:
FINISH:
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THIRD ANGLE PROJECTION
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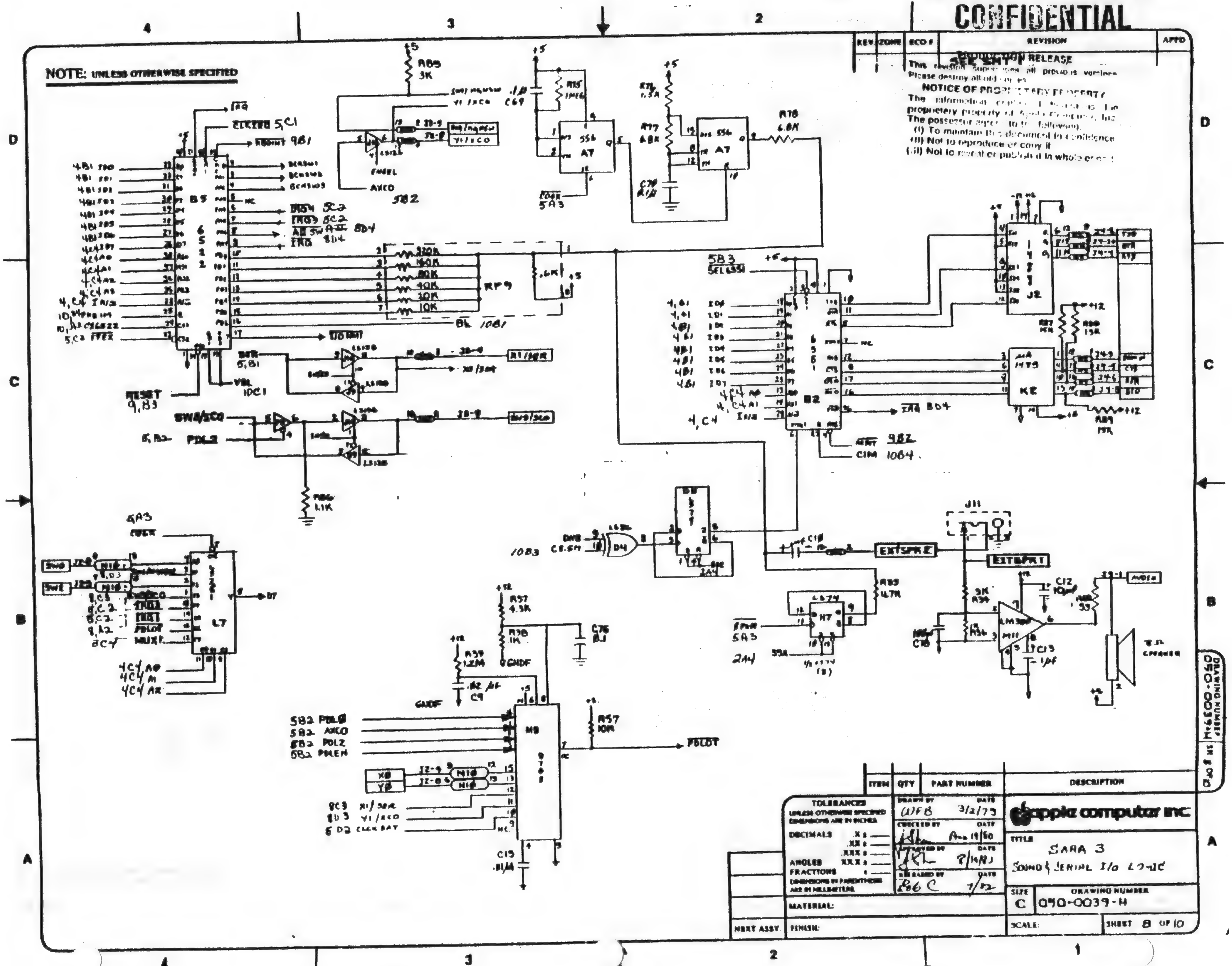
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REV. | ZONE | ECO # | REVISION | APPD
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6522
B5
556 A7
556 A7
RP9
6551
B2
1489
K2
1488
J2
LS74
H7
LM380
M11
J11
EXTSPKR
EXTSPKR
AUDIO
8 Ω SPEAKER
L7
M8
FSLOT
D4
B8
SW0
SW1
XØ
YØ
RESET 9,B3
SWØ/SCO
PDL2
R1/SER
ENSWI
IRQ
ITEM | QTY | PART NUMBER | DESCRIPTION
TOLERANCES
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DECIMALS .X ± .XX ± .XXX ±
ANGLES .XXX ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS
DRAWN BY WFB DATE 3/2/79
CHECKED BY DATE Aug 19/80
APPROVED BY DATE 8/14/80
RELEASED BY Bob C DATE 7/82
apple computer inc
TITLE SARA 3
Sound & Serial I/O Logic
SIZE C
DRAWING NUMBER 090-0039-H
MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET 8 OF 10
DRAWING NUMBER 090-0039-H SH 8 OF 10

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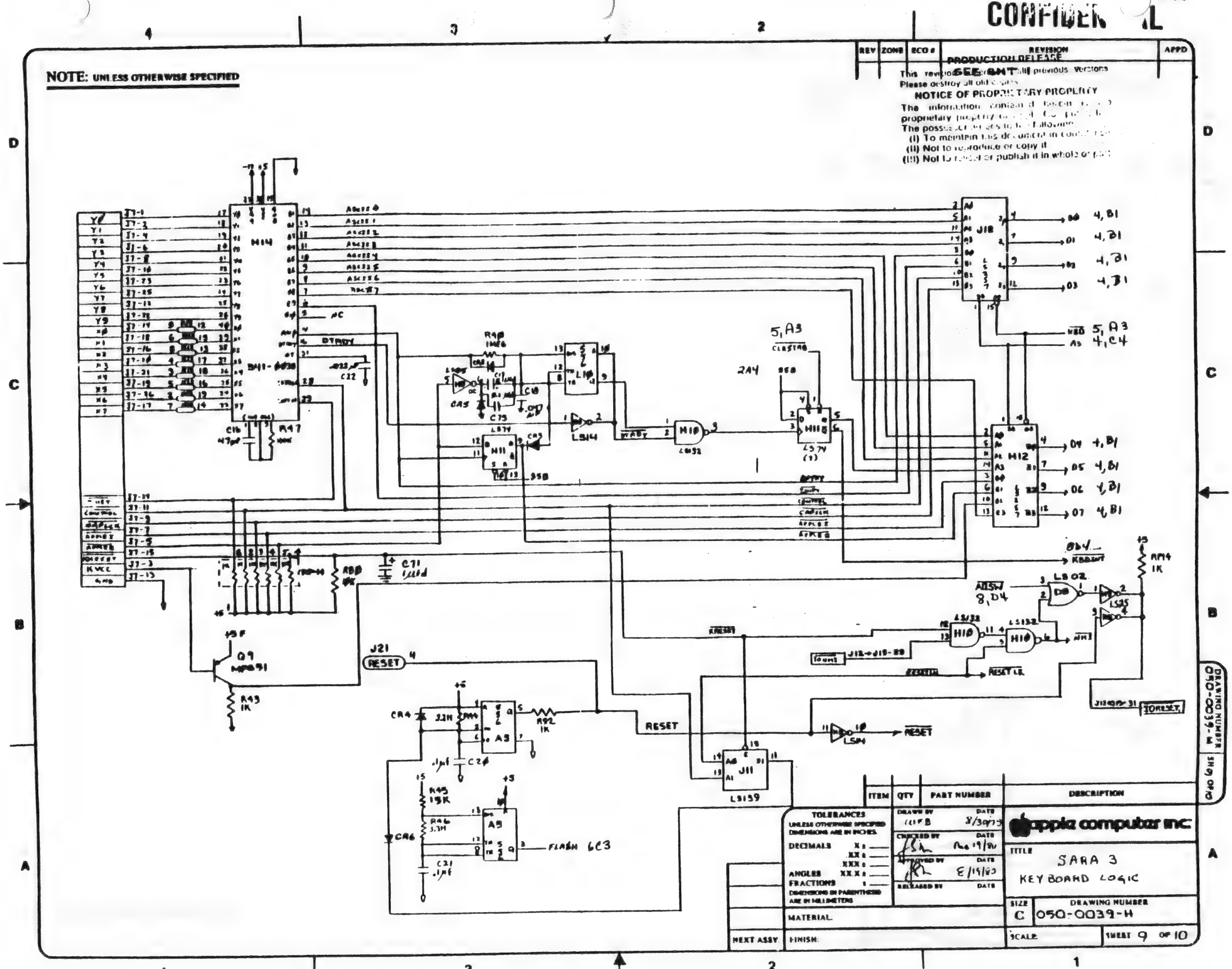

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REV
ZONE
ECO #
REVISION
APPD
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H14
J18
H12
H11
H18
H10
L18
J11
A5
A9
Q9
MPS51
R47
C16
47pf
C22
C71
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R88
R45
15K
R46
3.3M
R92
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R43
1K
RM4
1K
CR4
CR5
CR6
CR3
C21
.1µf
C24
.1µf
C19
C73
R48
J21
RESET
RESET
NC
DTRDY
ASCII 0
ASCII 1
ASCII 2
ASCII 3
ASCII 4
ASCII 5
ASCII 6
ASCII 7
D0 4,B1
D1 4,B1
D2 4,B1
D3 4,B1
D4 4,B1
D5 4,B1
D6 4,B1
D7 4,B1
5,A3
4,C4
5,A3
CLRSTRB
2A4
SSB
LS74
LS14
LS132
LS02
LS05
LS139
LS04
KBDINT
ADSW 8,D4
NMI
RESET LE
IORESET
J12-J15-30
FLASH 6C3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
X0
X1
X2
X3
X4
X5
X6
X7
CONTROL
KVCC
GND
J7-1
J7-3
J7-4
J7-6
J7-8
J7-10
J7-23
J7-25
J7-12
J7-22
J7-14
J7-18
J7-16
J7-20
J7-21
J7-19
J7-26
J7-17
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J7-13
+5
-12
+5F
ITEM
QTY
PART NUMBER
DESCRIPTION
TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS X ±
.XX ±
.XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS
DRAWN BY
CLFB
DATE
8/30/79
CHECKED BY
DATE
Au 19/80
APPROVED BY
DATE
8/19/80
RELEASED BY
DATE
MATERIAL:
FINISH:
NEXT ASSY.
apple computer inc
TITLE
SARA 3
KEYBOARD LOGIC
SIZE
C
DRAWING NUMBER
050-0039-H
SCALE
SHEET 9 OF 10
DRAWING NUMBER
050-0039-H
SH 9 OF 10

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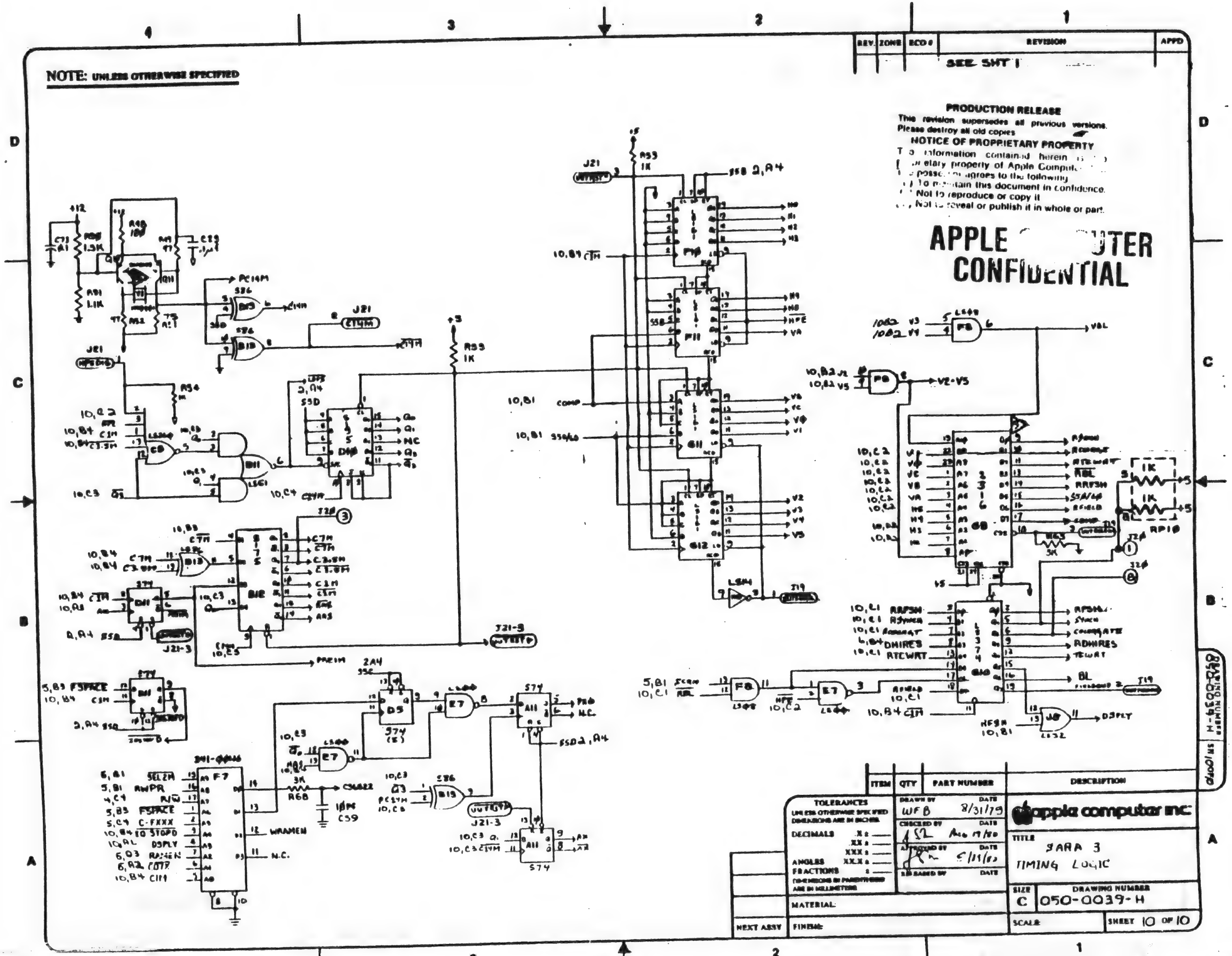

+12
C71 .01
R90 1.3K
R91 1.1K
R89 100
R92
C72 .1µf
PC14M
C14M
J21
C14M
C7M
J21
+5
R55 1K
R54
10,C2
10,B4 C3M
10,B4 C3.5M
10,C3 Q3
C8
LS260
B11
LS61
D14
Q0
Q1
NC
Q3
10,C4 C3HR
10,B4 C7M
10,B4 C3.5M
B13
B12
C7M
C3.5M
C1.0M
C3M
C3M
ARS
J28
J21-3
PRE1M
10,B4 CTM
D11
2,A4 S5D
5,B3 FSPACE
10,B4 C3M
B11
2,A4 S5D
341-0066
F7
5,B1 SELZM
5,B1 AWPR
4,C4 R/W
5,B3 FSPACE
5,C4 C-FXXX
10,B4 IO STOPD
10,A1 DSPLY
6,D3 RAMEN
6,A2 COTR
10,B4 C1M
WRAMEN
N.C.
3K
R68
CS6X2
10pF C59
2A4 S5C
D5
S74
E7
LS00
A11
PHO
N.C.
S5D 2,A4
10,C3 Q3
PC S7M 10,C8
B13
S86
J21-3
10,C3 Q
10,C3 C14M
A11
S74
J21
R53 1K
S5B 2,A4
10,B4 C1M
P10
P11
G11
G12
H0
H1
H2
H3
H4
H5
HPE
VA
VB
VC
VD
V1
V2
V3
V4
V5
10,B1 COMP
10,B1 S5/60
LS04
J19
1082 V3
1082 V4
F8
LS08
VBL
10,B2 V1
10,B2 V5
F8
V2•V5
3316
G8
RFSHM
RSYNCH
RTEWRT
RBL
RRFSH
S5A/60
RFIELD
COMP
J19
R65 3K
RP18
1K
1K
J28
10,C1 RRFSH
10,C1 RSYNCH
10,C1 RCOMPAT
6,B4 DHIRES
10,C1 RTEWRT
3374
G10
RFSH
SYNCH
COMPATE
RDHIRES
TEWRT
BL
J19
5,B1 SCRN
10,C1 RBL
F8
LS08
HPE 10,C2
E7
LS00
RFIELD 10,C1
10,B4 C1M
HFSH 10,B1
J8
LS32
DSPLY

REV. | ZONE | ECO # | REVISION | APPD

SEE SHT 1

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| ITEM | QTY | PART NUMBER | DESCRIPTION |
|---|---|---|---|

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES .XXX ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

DRAWN BY WFB DATE 8/31/79
CHECKED BY JSL DATE Aug 19/80
APPROVED BY JK DATE 5/11/82
RELEASED BY DATE

MATERIAL:
FINISH:
NEXT ASSY

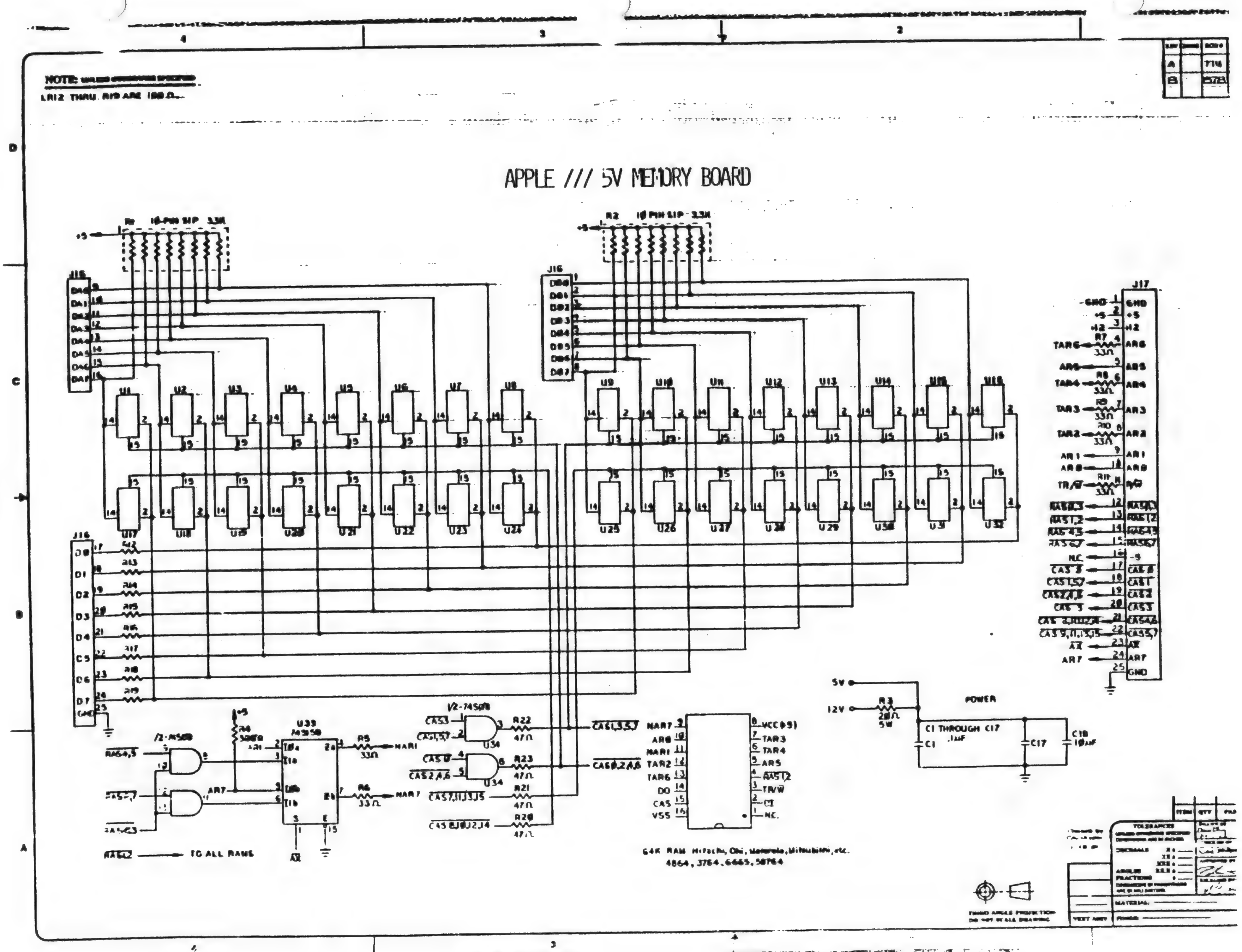
apple computer inc

TITLE SARA 3
TIMING LOGIC

SIZE C
DRAWING NUMBER 050-0039-H
SCALE:
SHEET 10 OF 10

DRAWING NUMBER 050-0039-H
SH 10 OF 10

# APPLE /// 5V MEMORY BOARD


NOTE:
LR12 THRU R19 ARE 100 Ω
R1 16-PIN SIP 3.3K
R2 16 PIN SIP 3.3K
+5
J15
DA0
DA1
DA2
DA3
DA4
DA5
DA6
DA7
J16
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
D0
D1
D2
D3
D4
D5
D6
D7
GND
R12
R13
R14
R15
R16
R17
R18
R19
J17
GND
+5
+12
AR6
AR5
AR4
AR3
AR2
AR1
AR0
R/W
RAS0,1
RAS1,2
RAS4,5
RAS6,7
-5
CAS0
CAS1
CAS2
CAS3
CAS4,6
CAS5,7
AX
AR7
TAR6
R7 33Ω
R8 33Ω
R9 33Ω
R10 33Ω
R11 33Ω
TAR4
TAR3
TAR2
TR/W
N.C.
CAS 0
CAS1,5,7
CAS2,4,6
CAS 3
CAS 0,10,12,14
CAS 9,11,13,15
1/2-74S08
RAS4,5
CAS5,7
RAS6,3
RAS0,2
TO ALL RAMS
R4 3000 Ω
U33 74S158
AR1
AR7
AX
R5 33Ω
R6 33Ω
NAR1
NAR7
1/2-74S08
CAS3
CAS1,5,7
CAS0
CAS2,4,6
U34
R22 47Ω
R23 47Ω
R21 47Ω
R20 47Ω
CAS7,11,13,15
CAS 8,10,12,14
CAS1,3,5,7
CAS0,2,4,6
NAR7
AR0
NAR1
TAR2
TAR6
DO
CAS
VSS
VCC(+5)
TAR3
TAR4
AR5
RAS1,2
TR/W
DI
N.C.
64K RAM Hitachi, Oki, Motorola, Mitsubishi, etc.
4864, 3764, 6665, 50764
5V
12V
R3 20Ω 5W
POWER
C1 THROUGH C17 .1μF
C1
C17
C18 10μF
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING
TOLERANCES
DECIMALS
ANGLES
FRACTIONS
MATERIAL
FINISH
A
B
C
D
1
2
3
4
714

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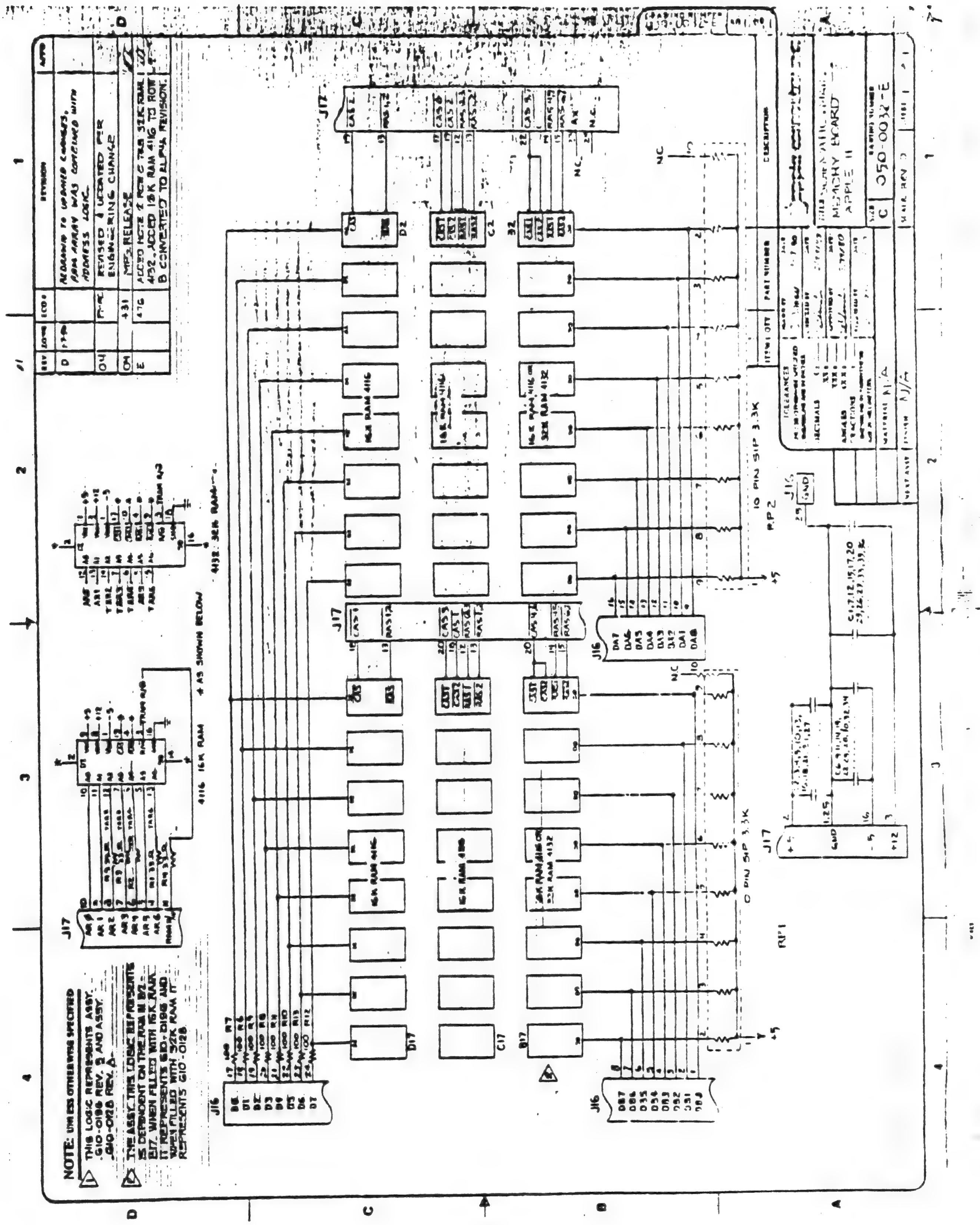

REV | ZONE | ECO # | REVISION | APPD
D | | | REDRAWN TO UPDATED CHANGES. PROM ARRAY WAS COMBINED WITH ADDRESS LOGIC.
04 | | P-P | REVISED & UPDATED PER ENGINEERING CHANGE
04 | | 431 | MP2 RELEASE
E | | 476 | ADDED NOTE 2 ROW C THRU 32K RAM 4132. ADDED 16K RAM 4116 TO ROW B CONVERTED TO ALPHA REVISION.
MEMORY BOARD
APPLE II
SIZE C
DRAWING NUMBER 050-0032-E
MATERIAL N/A
FINISH N/A
J17
J16
J15 GND
D2
C2
B2
D17
C17
B17
16K RAM 4116
16K RAM 4116 OR 32K RAM 4132
4116 16K RAM
4132 32K RAM
+ AS SHOWN BELOW
10 PIN SIP 3.3K
RP2
RP1
NC
+5
-5
+12
GND
NOTE: UNLESS OTHERWISE SPECIFIED
THIS LOGIC REPRESENTS ASSY. 610-0196 REV. 3 AND ASSY. 610-0126 REV. A.
THE ASSY. THIS LOGIC REPRESENTS IS DEPENDENT ON THE RAM IN B2-B17. WHEN FILLED WITH 16K RAM IT REPRESENTS 610-0196 AND WHEN FILLED WITH 32K RAM IT REPRESENTS 610-0126
1
2
3
4
A
B
C
D

# THE DISK /// SUBSYSTEM

## I THEORY OF OPERATION

The Disk /// subsystem, is a self contained Apple /// peripheral which allows user programs and data to be stored and retrieved on 5 1/4" floppy diskettes. The Apple /// supplies DC power, control signals, and a parallel data path to the Disk /// via the A///s main logic board Disk Conditioner (Controller) Circuit. The Disk Conditioner sends DC power, control signals, and serial data to the Analog Card via a 26-conductor ribbon cable.

The Analog Card contains disk read-write electronics, drivers for positioning Stepper Motor, and a transistor power switch. Analog Card also contains circuitry which causes its output signals to the disk conditioner circuit to be active only when the card is enabled. This allows up to 4 Analog Cards to share the same data path for a 4 drive system (one internal, three external drives).

Within the drive itself, movement of Stepper Motor rotates Actuator Cam. Head and Carriage Assembly's Cam Follower, rides in Actuator Cam's spiral groove. Two Guide Rods allow motion of Head and Carriage Assembly either towards, or away from Drive Door. This positions Read/Write Head to appropriate track, so that serial data may then be transferred to and from disk using high-level commands.

### A - DISK CONDITIONER CIRCUIT

There are seven sections in the Disk Conditioner circuit:
(Refer to Schematic of Disk Conditioner Logic)

1. Power-On Reset

This circuit consists of one half of 556 Timer and one open-collector inverter. When power is applied, the outputs of the 9334/LS259 Address Latch (DPh0-3) are brought low which places the Disk Conditioning logic in the read mode, the Q output of the 556 timer (pin 5) goes high for about 65 ms, bringing inverter's output to ground. This resets the State Machine (Prom P6A), and the Drive Enable Multiplexers. The drive enable multiplexer's Z output is prevented from enabling the internal and external drives.

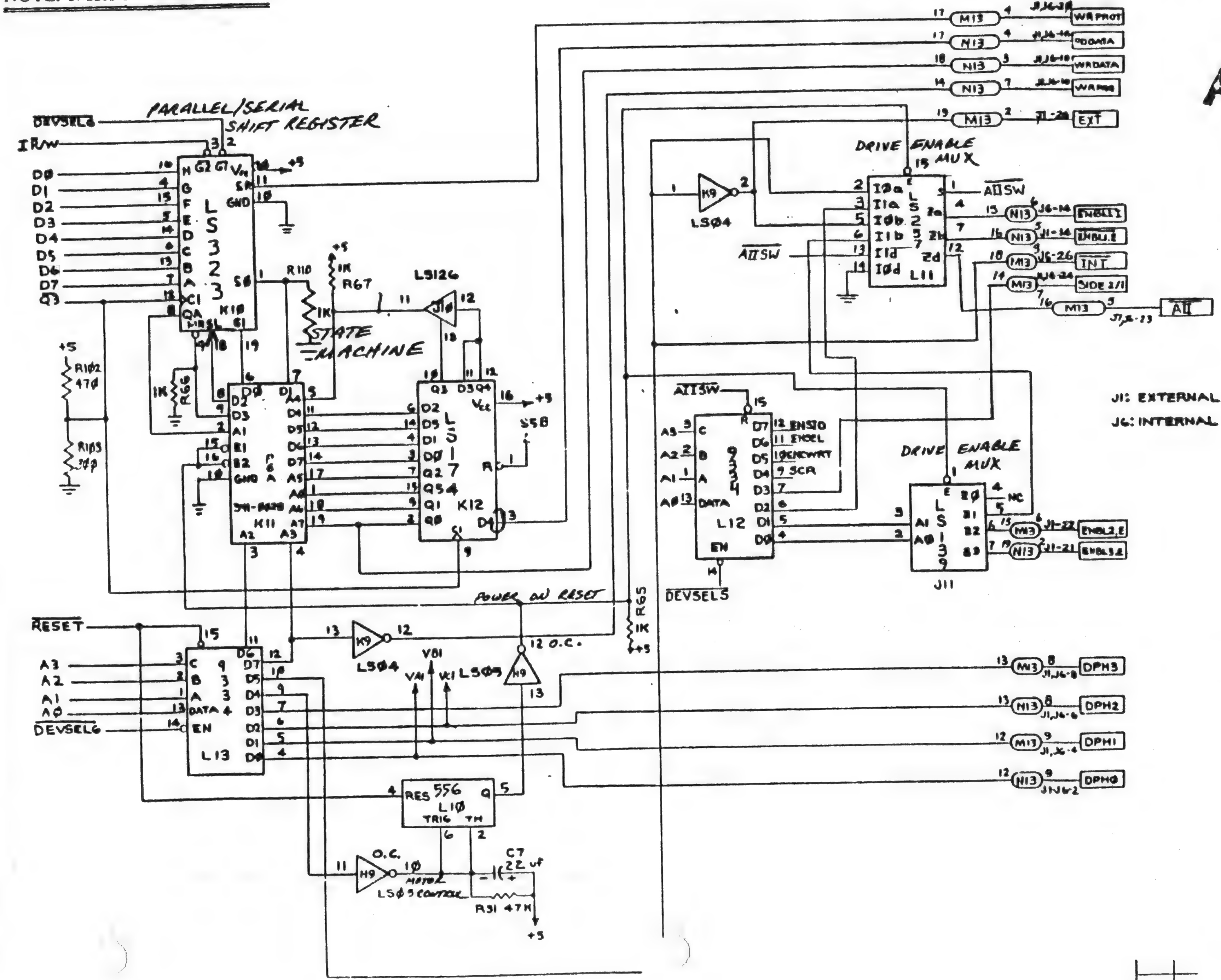
2. The BOOT ROM

The Boot ROM, though not a part of the disk conditioning circuit, contains the routine which down loads the operating system (SOS) from disk and then jumps into it. The LS323, an 8 Bit Parallel/Serial Register, is enabled (DEVSEL6*) whenever the address C0Exxn is presented. the data, from the boot rom, is converted to serial at the output of pin 1 in the 74LS323 in a write operation.

3. Addressable Latch (9334 or 74LS259).

| REV. | ZONE | ECO # | |
|---|---|---|---|
| G | | 778 | SEE SHT |

**NOTE:** UNLESS OTHERWISE SPECIFIED



PARALLEL/SERIAL SHIFT REGISTER
LS323 K10
DEVSEL6
IR/W
D0
D1
D2
D3
D4
D5
D6
D7
Q3
+5
R102 470
R103 390
R66 1K
R110
R67 1K
STATE MACHINE
LS126 J10
K11
LS174 K12
558
LS04 K9
A3
A2
A1
A0
A II SW
L12 9334
DATA
EN
DEVSEL5
EN SIO
EN SEL
ENWRT
SCR
DRIVE ENABLE 15 MUX
L11
DRIVE ENABLE MUX
LS139 J11
NC
M13
N13
WRPROT
RDDATA
WRDATA
WRREQ
EXT
ENBL1,I
INT
SIDE 2/1
A II
ENBL2,E
ENBL3,E
J1: EXTERNAL
J6: INTERNAL
POWER ON RESET
R65 1K
+5
RESET
L13 9334
DEVSEL6
LS04
V01
VA1
VK1
LS05 H9
O.C.
DPH3
DPH2
DPH1
DPH0
556 L10
RES
TRIG
TH
C7 22 uF
R31 47K
MOTOR LS05 CONTROL

APP
CO

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proprietary
The posses
(I) To mai
(II) Not to
(III) Not to r

This chip provides an eight software-controlled output. When DEVSEL6* (pin 9 of LS138 I/O Address Decoder) signal goes low (one of 16 addresses starting at [COExxn†, value of Address Line A0 becomes the new value of D output pointed to by Address Lines A1-A3. Latch output D6 and D7 set operating mode of controller (read, write, etc). Q5 selects the internal drive. D4 controls MOTOR ON signal and D0 to D3, set position of the Stepper Motor. Drive enable signals ENBL1I and ENBL1E are true when MOTOR ON signal is true and appropriate drive is selected.

4. State Machine (PROM P6A and 74LS174)

These two parts contain nucleus of Disk Conditioning Logic. A State Machine is a device capable of storing a value in a register. That value, in conjunction with external input, determines what the next register value should be and what output should be generated. Value in register is, machines's Current State and next value is machine's Next State. State machine updates at each clocking, going from state to state and producing output base on state its in and value of its input just before clocking.

Current State, is value at Q2, Q5, Q1, and Q0 from 74LS174. Next state is value of D4-D7 from P6A PROM. Input to State Machine includes D6 and D7 from 9334, QA* output from 74LS174 Shift Register and A2-11. Output from State Machine is PROM signals D0-D3, which effect Shift Register. Q0 from 74LS174, which is high-order bit of Current State, forms WR DATA output. Since State Machine is clocked by two Megahertz Q3* signal, the state lasts for 500 ns.

Flux transitions on diskette are detected by Analog Card and are sent to Disk Conditioning Circuitry as RD DATA. These one microsecond positive going pulses appear at D4 input to 74LS174. NAND Gate and Inverter, which connect to 74LS174's Q3 and Q4 output, cause A4 input to P6A PROM to go low for one state following the falling edge of RD DATA. This information is ignored when writing out to disk. When reading from disk, however, this input forms the basis for determining whether a logic one or zero has been read. A logic one is indicated by a four microsecond period. A logic zero, by an eight microsecond period between flux transitions.

5. Shift Register

74LS323 Universal 8 Bit Parallel/Serial Shift Register, transfers data to and from the Apple ///. When writing to disk, Shift Register under control of State Machine, parallel loads a data byte from the A/// and shifts it left. This causes QA* output to effect State Machine's A1 input. State Machine goes through a different state sequence for a logic one and a logic zero, which causes WR DATA to change value every four and eight microseconds, respectively.

When reading from disk, State Machine shifts appropriate logic levels into Shift Register's SL input. Resulting byte can be read by the A///.

Status of Write Protect switch in Disk Drive, comes into SR input of

Shift Register from Analog Card. Under control of State Machine, Shift Register is placed into a shift right mode, allowing status of switch to be read by software.

6. MOTOR ON Circuit.

Q output from one half of 556 timer, forms MOTOR ON signal. MOTOR ON becomes true when B2-6 is brought to ground under software control. An enable is sent to one of the drives, and Drive Motor in selected drive turns on. When software causes B2-6 to become high-impedance in order to turn off drive, C7 and R31 give drive a 2/3 second grace period before MOTOR ON times out. This prevents drive from being turned on and off when repeated accesses are made.

7. AII EMULATION MODE

With the AIISW* true and DEVSEL5* (addressed by C0Dxxn) selected, the internal and external drives are fooled into operating as an Apple II Disk Drive.

## B - ANALOG CARD (Refer to Analog Card Schematic Diagram)

1. Enable Circuit

A Disk Drive connected to the Apple /// is always in one of three operating modes:

a - Read Mode

Flux transitions on diskette are detected by MC3470P Floppy Disk Read Amplifier on Analog Card and are sent to the Disk Conditioner as one microsecond positive-going pulses across RD DATA* line.

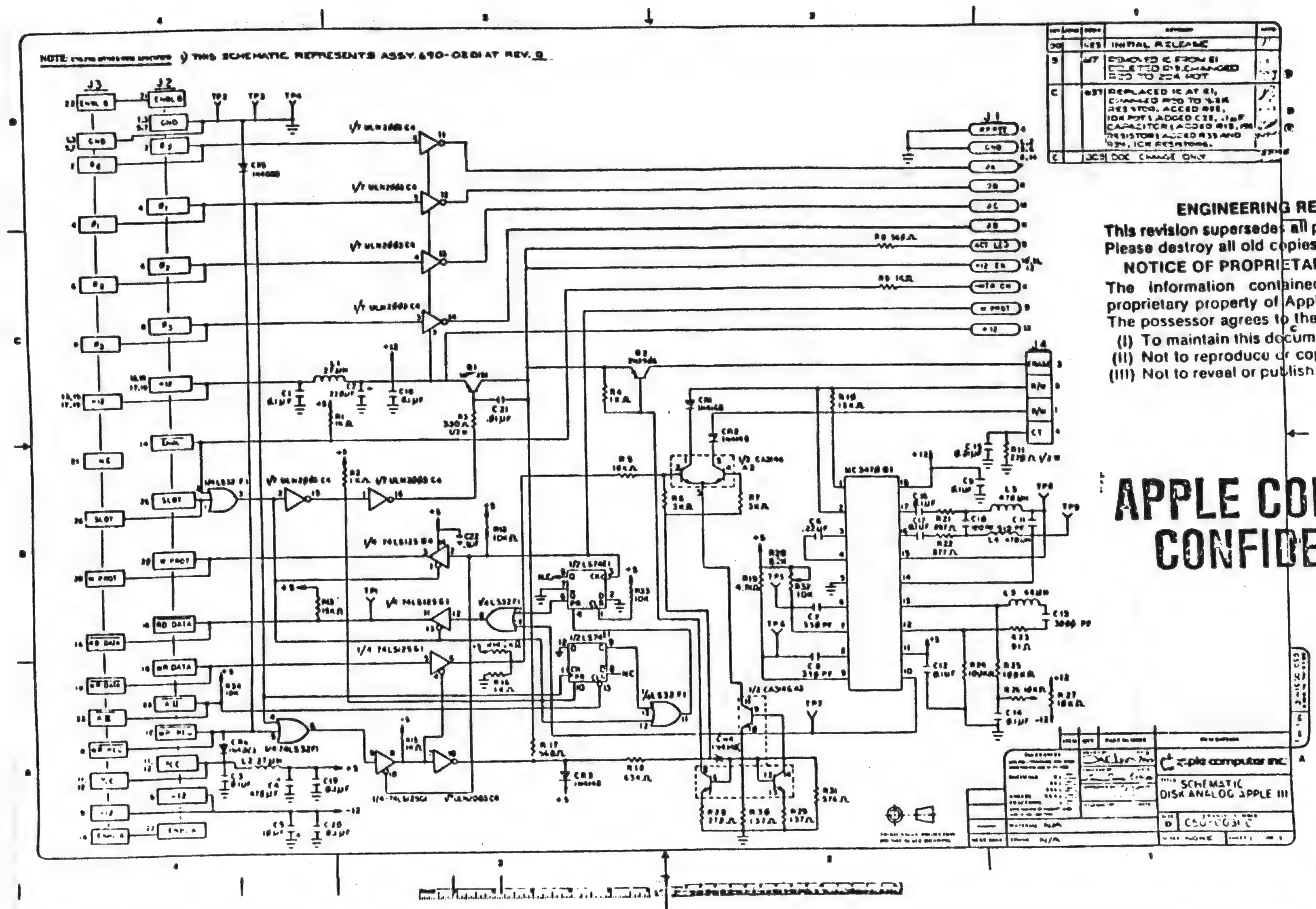
b. Write Mode

Here WR DATA input to Analog Card determines polarity of write current passing through head.

c. Deselected Mode

In this state, drive is not currently performing any data transfers with the Apple ///.

A drived becomes enabled, when ENBL1I input to the Analog Card on the selected drive goes low. This causes Q1 to turn on because current flows through R3 into pin 16 of ULN2003's Darlington output. +12 volts is then supplied to Stepper Motor. Q1 also provides a power source for Write and Erase Current circuits. In addition, ENBL1I signal also enable RD DATA* and W PROT tristate buffers and supplies a MTR ON control signal to Motor Control Board through resistor R9.


NOTE: 1) THIS SCHEMATIC REPRESENTS ASSY. 690-0201 AT REV. 0
J3
J2
J1
J4
TP2
TP3
TP4
1/7 ULN2003C4
1/4 74LS125
1/2 LS74
1/4 74LS32
MC3470
1/2 CA3046
RD DATA
WR DATA
SLOT
W PROT
INITIAL RELEASE
REMOVED C FROM E1 DELETED R19, CHANGED R20 TO 20K POT
REPLACED IC AT E1, CHANGED R20 TO 8.2K RESISTOR, ADDED R32, 10K POT | ADDED C22, .1 µF CAPACITOR | ADDED R13, RESISTOR | ADDED R33 AND R34, 10K RESISTORS.
DOC CHANGE ONLY
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SCHEMATIC
DISK ANALOG APPLE III
D
N/A
NONE

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d. Read Electronics

MC3470P Floppy Disk Read Amplifier and associated discrete components, provide a one-chip interface between magnetic head of Disk Drive and RD DATA* input to Disk Conditioning circuit of the main logic board. MC3470P contains both analog and digital circuits which cause a TTL compatible pulse to be generated for each positive and negative peak of input signal.

Input voltage from head appears across pins 1 and 2 of MC3470P. This signal passes through an amplifier and is differentially applied to a noise filter made up of R21 and R22, C10 and C11 and L3 and L4. Filter's output feeds back into MC3470P, where a differentiator circuit provides an output proportional to rate of change, with time, of input signal. In addition, a 90 degree phase lead is introduced which causes a zero crossing at differentiator's output to correspond with a peak at its input. L5, C13 and R23 determine characteristics of differentiator. R27 allows for correction of current imbalances within differentiator so that a sinusoidal input waveform produces evenly spaced RD DATA* pulses.

Zero crossings at output of differentiator cause output of a comparator within MC3470P, in conjunction with digital circuits, create a Time Domain Filter which checks against false zero crossing readings due to distored input waveforms or noise. When a zero crossing is detected, mono #1, formed by R20, R32, and C7, is triggered. At end of its two microsecond period, output of comparitor is again checked. If it has not changed (valid zero - crossing), mono #2 gets a trigger pulse that uses R19 and C8 to generate one microsecond RD DATA* pulse at pin 10 of MC34709P.

3. Write Electronics

During Read Mode (WR REQ* high), ULN2003 Darlington output at C4-10, is close to ground potential. This prevents erase current switch Q2 from turning on and disables write current return path. During Write Mode, the anode of CR3 is pulled up to +5.7 V. Q2 receives base current through A3-8, and provides current to erase coil of head. R11 serves as return for erase current, which is roughly 44 milliamps. Erase coil in head straddles both sides of read-write head, preventing write current from spreading into adjacent tracks on diskette.

When writing out to diskette, flux transistions are placed on surface of diskette by changing polarity of current flow in head's read-write coil. Write current enters read-write coil through its center tap, which is connected to return side of erase coil. Two of CA3146's transistors connected to R29 and R30 form a current mirror which drives pin three of CA3146.

This establishes write current return path. When writing out to disk, WR DATA causes a differential voltage to be applied to pins 2 and 4 of CA3146, which causes a differential current flow in write coil. Each polarity reversal places a flux reversal on diskette. (Current in R/W coil -6.8 ma P-P)

## 4. Write Protect Circuit

Ananlog Card only allows erase and write current to be generated when diskette has its write protect notch uncovered. If notch is absent (write protected), the Write Protech switch is held open even though diskette is fully inserted into drive. This causes pullup resistor R12 to disable G1-8, which causes WR REQ* signal to be pulled up to a false level by R15. This prevents write current mirror from supplying write current to head. Write Protect status is ent to Disk Conditioning circuitry on Main Logic board as W PROT.

If Write Protect notch has been uncovered, it cause Write Protect switch within drive to close. Phase 1 signal from the Disk Conditioning circuitry provides return path for current passing through switch. If Phase 1 signal is high, it indicates that Stepper Motor is in one of its two transient states between tracks. Write Protect circuits behave as they do when the diskette is write protected. This provides partial coverage against writing when Stepper Motor is off track.

## 5. Stepper Motor Drivers

A ULN2003 Darlington Buffer-Inverter, provides a current return path for each of four Steper Motor windings, Phase A through Phase D. Q1 provides windings with source current when dirve is enabled. Since input to each ULN2003 stage is provided by the Disk Conditioning circuit's 9334 Addressalbe Latch output, Stepper Motor is then under software control.

Stepping in from Track 0 towards Track 34 (towards hub), requires Stepper Windings to be energized in Phase A, B, C, D order. Each phase rotates Cam Follower enough to provide one-half track movement of Head and Carriage assembly. Phase Ad and C are energized when head is on track, and Phase B and D are between track positions. Once head is positioned to desired track, power is removed from Stepper Motor to reduce power consumption.

Stepping out requires Stepper Motor windings to be enegized in Phase D, C, B, A order. When booting, windings are pulsed enough times to guarantee that head is positioned over Track 0.

NOTE:

1. THESE ITEMS ARE SUPPLIED WITH O.E.M. DISK DRIVE (ITEM 2).
2. ITEM 12 (CARRIAGE LOCK CARD) TO BE INSERTED AFTER UNIT IS ASSEMBLED.

| | | | | |
|---|---|---|---|---|
| 00 | | | INITIAL RELEASE | |
| B | | | ADDED ITEM 12, NOTE 2 & DETAIL A. | |

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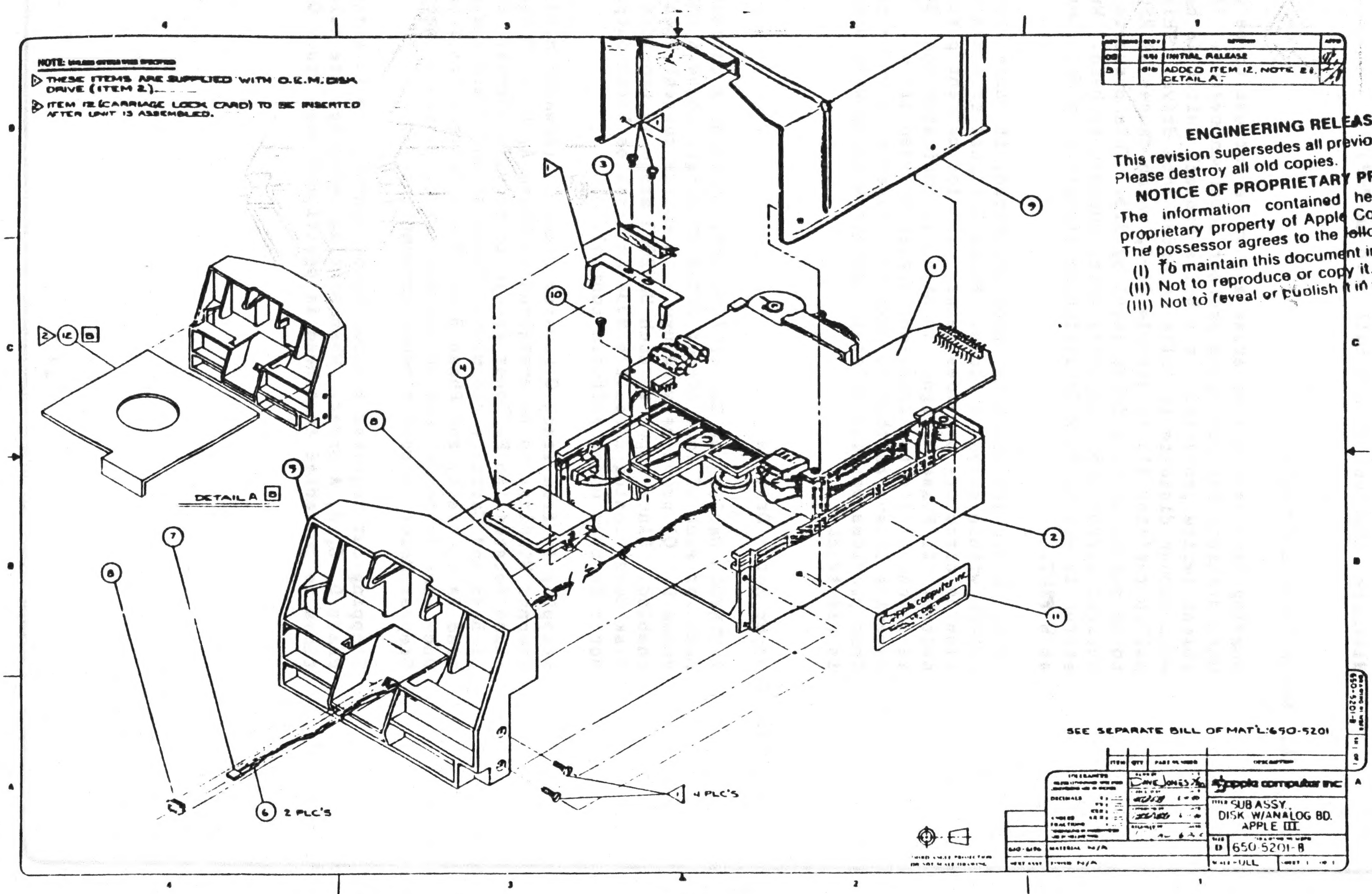

SEE SEPARATE BILL OF MAT'L: 650-5201

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TITLE SUBASSY.
DISK W/ANALOG BD.
APPLE III

D 650-5201-B

MATERIAL N/A

FINISH N/A

Dave Jones

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DOCUMENT NO. 064-0156

PAGE 5 OF 14

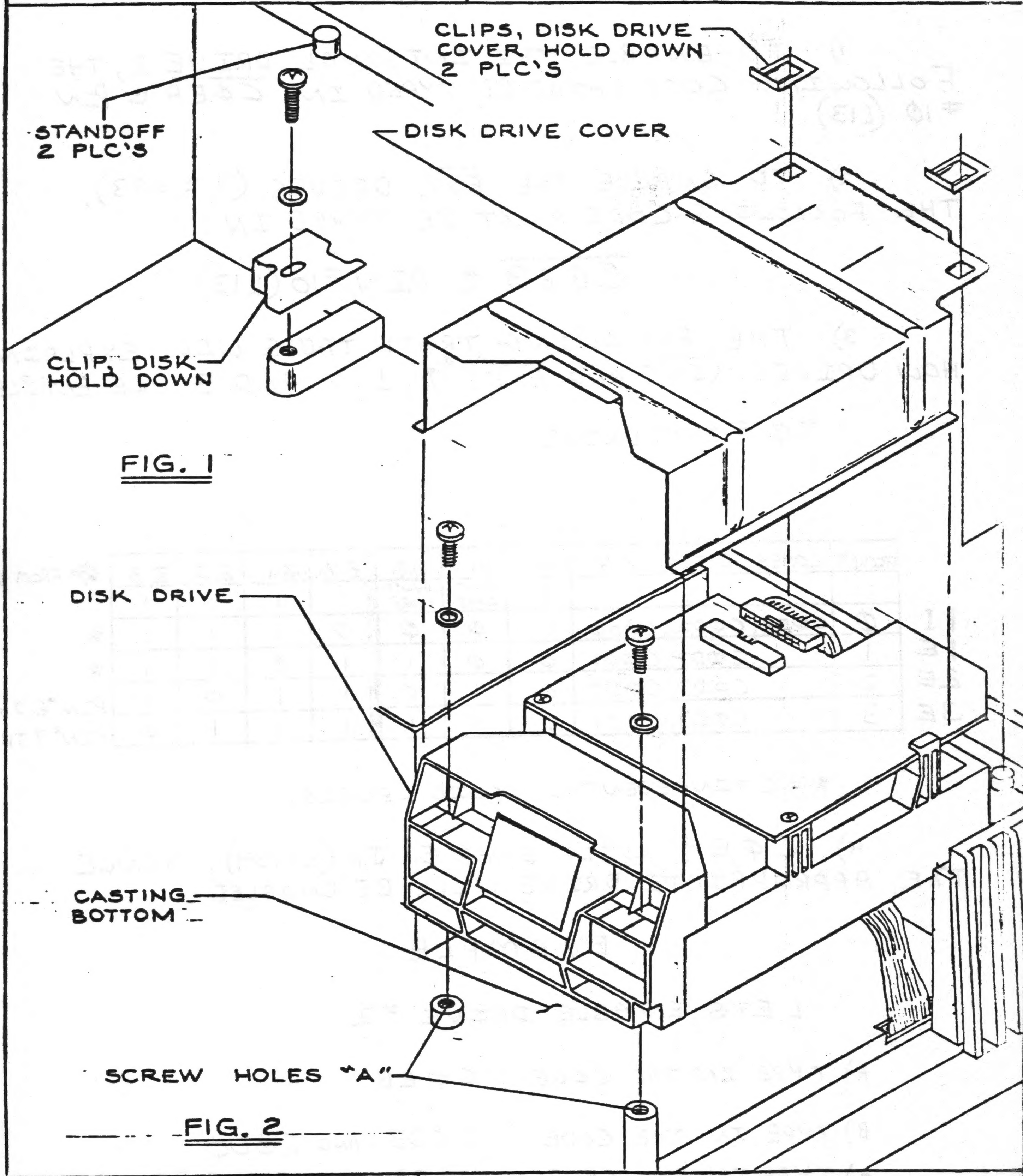
CLIPS, DISK DRIVE COVER HOLD DOWN 2 PLC'S
STANDOFF 2 PLC'S
DISK DRIVE COVER
CLIP, DISK HOLD DOWN
DISK DRIVE
CASTING BOTTOM
SCREW HOLES "A"

FIG. 1

FIG. 2

| DRAWN BY | OPERATION NO. | TITLE |
|---|---|---|
| | 010 | INSTALL DISK DRIVE |

# APPLE III

## DISK ENABLE(S)

1) TO ENABLE THE INTERNAL DRIVE 1, THE FOLLOWING CODE SHOULD BE TYPED IN: $\overline{C0EA}$ @ PIN #10 (L13)

2) TO ENABLE THE $\overline{EXT.}$ DRIVES (1, 2, OR 3), THE FOLLOWING CODE MUST BE TYPED IN:

$\overline{C0EB}$ @ PIN #10 (L13)

3) THE FOLLOWING TRUTH TABLE WILL EXPLAIN HOW DRIVES ($\overline{INT}$ AND $\overline{EXT}$) *0, 1, 2 AND 3 ARE ENABLED

*0 ≡ INT. DRIVE

| | DRIVE # | CODES TO TYPE IN | ENABLE | A1 | A0 | Z0 | Z1 | Z2 | Z3 | ➡ FROM J11 (L |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | DON'T CARE | DON'T CARE | 1 | 1 | 1 | 1 | |
| 1 I | 0 | C0D4, C0D2, C0D0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | ★ |
| 1 E | 1 | C0D2, C0D1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | ★ |
| 2E | 2 | C0D3, C0D0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | PIN #6 J11 (LS139) |
| 3E | 3 | C0D3, C0D1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | PIN #7 J11 (LS139) |

★ ≡ COINCEDENTAL LOGIC LEVELS.

4) C0E9 WILL ENABLE J11 (LS139), HENCE THE APPROPRIATE DRIVE WILL BE ENABLED.

EXAMPLE:

LETS ENABLE DRIVE #2

A) TYPE IN THE CODE: C0EB

B) TYPE IN THE CODE: C0D3 AND C0D0

C) TYPE IN THE CODE: C0E9 NOW DRIVE #2 IS ON

D) TYPE IN THE CODE: C0E8 NOW DRIVE #2 IS OFF.

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S. WOITH